SIEMENS

Microcontrollers

Data Catalog

SIEMENS

Microcontrollers

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General Informations

8-Bit Single-Chip Microcontrollers

General Information

1. Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15[1)], edition 1988.

2. Mounting Instructions

Plastic Packages for Insertion

The pins of the packages are bent downwards by an angle of 90° and fit into holes on a grid of 2.54 mm and with diameters of between 0.7 and 0.9 mm. The dimension x is shown in the corresponding drawing of the package.

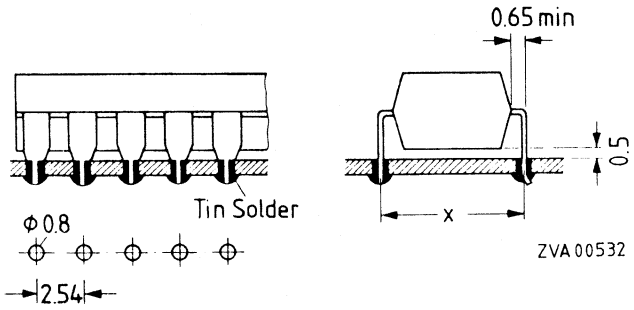
The bottom of the package will not touch the circuit board after insertion because the pins have shoulders just below the package (see **figure 1**).

After insertion of a package on a board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering.

Plastic packages are soldered on the board on the side facing away from the package.

The maximum permissible soldering temperature is 260 °C (max. 10 s) when using a solder bath, e.g. wave soldering, and 350 °C (max. 3 s) when using a soldering iron.

Figure 1



Dimensions in mm

Plastic Packages (P-DSO and P-LCC) for Surface Mounting (SMD)

Reflow soldering: for a device temperature of 215 °C max.,
soldering time 2 × 40 s (typical figure for vapor-phase soldering)

Wave soldering: soldering temperature 260 °C,
soldering time max. 10 s

1) Available from Pro Electron, Avenue Louise, 430 (B.12), B–1050 Bruxelles, Belgium

Soldering iron: the minimum thermal stress, based on experience, is at a soldering temperature of 350 °C (soldering time ≤ 3 s)

Storage and Pretreatment of SMD ICs

The components should be stored in a dry place. Some large and specially identified plastic ICs have to be processed in a dry condition. This is produced by dry packing or by means of a separate drying process shortly before they are processed (e.g. 16 h at 125 °C).

3. Processing Guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics. MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to 10^9 Ω).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer

ZVL00139

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 Ω/cm.

3. With humidity of > 50 % a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 kΩ to 100 kΩ.
4. If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^5 to 10^8 Ω.
6. When loading machines and production devices it is necessary to ensure that the devices do not come out of the transport magazine charged and that they are not damaged by touching metal, e.g. parts of a machine.

   Example 1: conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person. Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2: anti-static (transparent) tubes.
   The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be engangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material (≈ 10^6 to 10^8 Ω/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminium – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose.

During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 30 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ... -B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical Tests and Application Circuit

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting ring.
2. The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or with drawn, unless works' specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has first to be connected. In general, an interruption of this potential during operation is not permissible.
4. Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
5. Power supplied of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.

   Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplied, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered.

   When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, dioderior to the load rejection should be taken into account.
6. ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN endstages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.
7. Observe any notes and instructions in the respective data books.

Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity: $10^5\ \Omega/cm < p < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40 % — this requirement is fulfilled by a simple corrugated board.

Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

You should always ensure that different boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example.

For this purpose a sheath of aluminium foil is recommended, although direct contact between the film and the PCB must be avoided.

Cardboard boxes with an aluminium-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t < 2 min
alternating sound pressure	p < 29 kPa

4. Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5. Quality Assurance

Quality Assurance System

The high quality and reliability of integrated circuits from Siemens are the results of carefully managed design and production which is systematically checked and controlled at each stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Quality Assurance – Integrated Circuits".

Figure 1 and 2 show the most important stages of Quality Assurance (QA) system. QA departments independent of production and development are responsible for the selected measures, acceptance procedures and information feedback loops. Operating QA departments have state-of-the-art test and measuring equipment at their disposal, work according to approved methods of statistical quality control, and are provided with facilities for accelerate life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The QA department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives to ensure statistically that the PDA of released lots is less than the AQL agreed. Sampling inspection is performed in accordance with the inspection plans of DIN 40 080, as well as of the identical MIL-STD-105 or IEC 410.

Figure 2

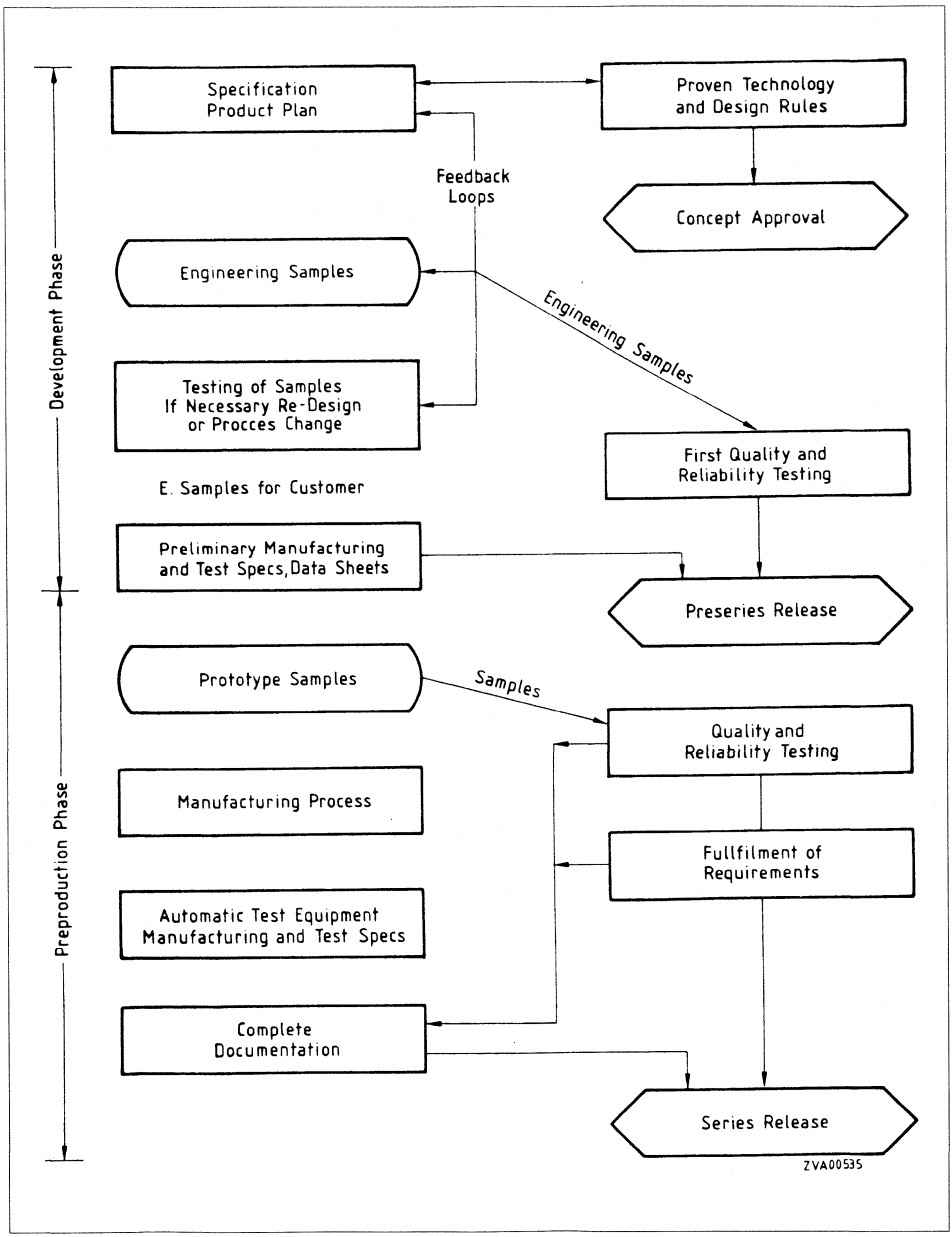
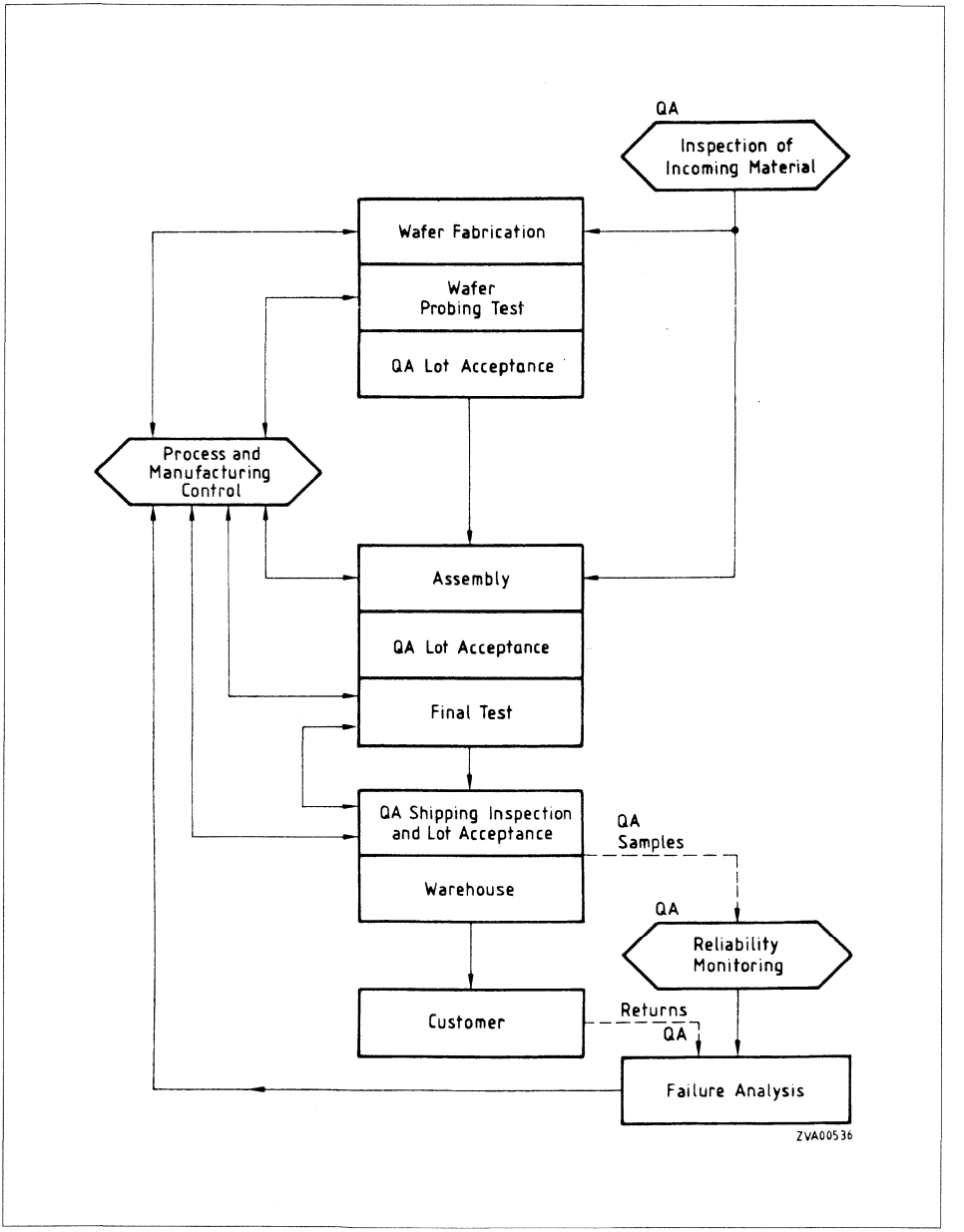

Development Phase
Preproduction Phase
Specification
Product Plan
Proven Technology
and Design Rules
Feedback
Loops
Concept Approval
Engineering Samples
Engineering Samples
Testing of Samples
If Necessary Re-Design
or Procces Change
First Quality and
Reliability Testing
E. Samples for Customer
Preliminary Manufacturing
and Test Specs, Data Sheets
Preseries Release
Prototype Samples
Samples
Quality and
Reliability Testing
Manufacturing Process
Fullfilment of
Requirements
Automatic Test Equipment
Manufacturing and Test Specs
Complete
Documentation
Series Release
ZVA00535

Figure 3


QA
Inspection of Incoming Material
Wafer Fabrication
Wafer Probing Test
QA Lot Acceptance
Process and Manufacturing Control
Assembly
QA Lot Acceptance
Final Test
QA Shipping Inspection and Lot Acceptance
QA Samples
Warehouse
QA
Reliability Monitoring
Customer
Returns
QA
Failure Analysis
ZVA00536

Reliability

Measures Taken During Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, e.g. specifying minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these designs standards.

In-Process Control During Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-progress control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged in a manner that the individual steps of the process can be reproduced continuously.

The decreasing failure rates reflect the persistent effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in IC complexity.

Reliability Monitoring

The general course of the IC failure rate versus time is shown by a so-called "bathtub" curve. The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data gained from life tests are converted to an operating temperature of $T_A = 55$ °C, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 22, compared with operational behavior. This method also considers failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "Quality Assurance-Integrated Circuits". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker text, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

6. Summary of the Most Important Symbols

b	Pulse duration
B	Current gain
B	Bandwidth
BI	Input of output amplifier
BO	Output of output amplifier
C	Capacitance
C_I	Input capacitance
$C_{I\,CLK}$	Input capacitance of the clock input
C_L	Load capacitanc
D	Data input
DO	Data output
E	Enable
F_I	Input load factor
F_O	Output load factor
F_{OH}	Output load factor, H signal
F_{OL}	Output load factor, L signal
f_I	Input frequency
$f_{CL}, f\phi$	Clock frequency
f	Maximum counter frequency
I_{DD}	Drain supply current
I_I	Input current
I_{IH}	H-input current
I_{IL}	L-input current
I	Input
I1	Input 1
I2	Input 2
I	Input bias current
I_{OO}	Output offset current
I_O	Short-circuit output current
I_{OH}	H-output current
I_{OL}	L-output current
I_{SH}	H-supply current
I_{SL}	L-supply current
MO	Mixer output
0 s, GND	Ground, earth
P_{tot}	Total power consumption
P_O	Output power
CLK	Clock
O	Output
$\overline{O}$	Output inverted

R	Resistance
R_G	Generator resistance
R_I	Input resistance
R_{CL}	Collector load resistance
R_L	Load resistance
R_P	Adjustment resistance
$R_{th\ JA}$	Therminal resistance (Junction to ambient)
R_{OH}	H-output resistance
R_{OL}	L-output resistance
R_O	Load resistance at output
T_A	Ambient temperature
T_{stg}	Storage temperature
T_{case}	Case temperature
T_j	Junction temperature
TC	Temperature coefficient
t_d	Pulse delay time
$t_{DHL\ O}$	Delay time of the HL transition of the output signal
$t_{DLH\ O}$	Delay time of the LH transition of the output signal
t_{DLH}	Delay time
t_H	Hold time
t_I	Input pulse duration
t_n	Bit time before clock pulse
t_{n+1}	Bit time after clock pulse
t_P	Average signal propagation time
t_{SYD}	Delay time
t_{CLKY}	Clock period
t_{PHL}	Signal propagation time (from H to L)
$t_{PHLR,S}$	Signal propagation time (set, reset input)
t_{PD}	Pair-delay time
t_{pR}	Reset pulse duration
$t_{PR,S}$	Average signal propagation time (set, reset input)
t_{pS}	Set pulse duration
t_d	Key debounce time
t_p	Key depression period
t_{pC}	Counting pulse duration
t_T	Transmission time – t_r rise time, t_f fall time
t_r	Recovery time
t_S	Setup time
t_O	Output pulse duration
t_{THL}	Signal transition time (from H to L)
t_{TLH}	Signal transition time (from L to H)
$t_{THL\ O}$	Signal transition time H-L of the output signal
$t_{TLH\ O}$	Signal transition time L-H of the output signal

7. Abbreviations

ACFA	Advanced CMOS Frame Aligner
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
B8ZS	Bipolar Eight Zero Substitution coding
CAS	Channel Associated Signaling
CAS-CC	CAS Common Channel
CAS-BR	CAS Bitrobbing mode
CCS	Common Channel Signaling
CRC	Cyclic Redundancy Check
CRC4	CRC using four check bits
CRC6	CRC using six check bits
DL	Data Link bits
DMA	Direct Memory Access
E bits	similar to Si*-bits
ESF	Extended Superframe (24-frame multiframe, PCM 24)
F4	4-frame multiframe structure (PCM 24)
F12	12-frame multiframe structure (D3/D4, PCM 24)
F72	72-frame multiframe structure (Remote Switch Mode, PCM 24)
FAS	Frame Alignment Signal
FDL	similar to DL
FS	Service bits, in F12 and F72 format also containing the multiframe alignment signal
FT	Terminal Framing bits defining the pulseframe position in F4, F12, and F72 format
HDB3	High Density Bipolar Three zero maximum coding
HDLC	High Level Data Link Control Procedure
HSCX	High Level Serial Communication Controller Extended (SAB 82525)
IPAT®	ISDN Primary Access Transceiver (PEB 2235/PEB 2236)
MTSC	Memory Time Switch CMOS (PEB 2045)
NOS	No Signal alarm
NRZ	Non Return to Zero signal
$\mathbf{S}_a$	similar to S_n bits
S_i bits	Spare bits for international use (PCM 30, Doubleframe format)
S_i* bits	Spare bits for international use (PCM 30, CRC Multiframe format)
S_n bits	Spare bits for national use (PCM 30)
TS ..	Time slot ..
UI	Unit Interval
ZCS	Zero Code Suppression

Summary of Types (incl. ordering codes)

Summary of Types

Type	Ordering Code	Package	Descriptions	Page
8-Bit Single-Chip Microcontrollers				
SAB 8031A-P-T40/85	Q 67120-C230	P-DIP-40	for external memory, 12 MHz, ext. Temp.	33
SAB 8031A-P	Q 67120-C183	P-DIP-40	for external memory, 12 MHz	33
SAB 8031A-N	Q 67120-C271	P-LCC-44		
SAB 8031A-16-P	Q 67120-C347	P-DIP-40	for external memory, 16 MHz	33
SAB 8031A-16-N	Q 67120-C349	P-LCC-44		
SAB 8031A-20-P	Q 67120-C466	P-DIP-40	for external memory, 20 MHz	33
SAB 8031A-20-N	Q 67120-C467	P-LCC-44		
SAB 8051A-P-T40/85	Q 67120-C233	P-DIP-40	with 4-KByte mask-programmable ROM 12 MHz, ext. Temp.	33
SAB 8051A-P	Q 67120-C186	P-DIP-40	with 4-KByte mask-programmable ROM 12 MHz	33
SAB 8051A-N	Q 67120-C224	P-LCC-44		
SAB 8051A-16-P	Q 67120-C346	P-DIP-40	with 4-KByte mask-programmable ROM	33
SAB 8051A-16-N	Q 67120-C348	P-LCC-44	16 MHz	33
SAB 8051A-20-P	Q 67120-C489	P-DIP-40	with 4-KByte mask-programmable ROM	33
SAB 8051A-20-N	Q 67120-C490	P-LCC-44	20 MHz	33
SAB 8032B-P	Q 67120-C419	P-DIP-40	for external memory, 12 MHz	53
SAB 8032B-N	Q 67120-C423	P-LCC-44		
SAB 8032B-P-T40/85	Q 67120-C427	P-DIP-40	for external memory, 12 MHz, ext. Temp.	53
SAB 8032B-16-P	Q 67120-C421	P-DIP-40	for external memory, 16 MHz	53
SAB 8032B-16-N	Q 67120-C425	P-LCC-44		
SAB 8032B-20-P	Q 67120-C471	P-DIP-40	for external memory, 20 MHz	53
SAB 8032B-20-N	Q 67120-C472	P-LCC-44		
SAB 8052B-P	Q 67120-C420	P-DIP-40	with 8-KByte mask-programmable ROM, 12 MHz	53
SAB 8052B-N	Q 67120-C424	P-LCC-44		
SAB 8052B-P-T40/85	Q 67120-C428	P-DIP-40	with 8-KByte mask-programmable ROM 12 MHz, ext. Temp.	53

Summary of Types (cont'd)

Type	Ordering Code	Package	Descriptions	Page
SAB 8052B-16-P	Q 67120-C422	P-DIP-40	with 8-KByte mask-programmable	53
SAB 8052B-16-N	Q 67120-C426	P-LCC-44	ROM, 16 MHz	53
SAB 80513-P	Q 67120-C383	P-DIP-40	with 16-KByte mask-programmable	53
SAB 80513-N	Q 67120-C384	P-LCC-44	ROM, 12 MHz	53
SAB 80513-16-P	Q 67120-C441	P-DIP-40	with 16-KByte mask-programmable ROM, 16 MHz	53
SAB 80515-N	Q 67120-C211	P-LCC-68	with mask-programmable ROM	75
SAB 80535-N	Q 67120-C241	P-LCC-68	for external memory	75
SAB 80515-N-T40/85	Q 67120-210	P-LCC-68	with mask-programmable ROM	75
SAB 80535-N-40/85	Q 67120-240	P-LCC-68	for external memory	75
8-Bit CMOS Microcontroller				
SAB 80C515-N	Q 67120-C297	P-LCC-68	with mask-programmable ROM, 12 MHz	113
SAB 80C535-N	Q 67120-C508	P-LCC-68	for external memory, 12 MHz	113
SAB 80C515-N-T40/85	Q 67120-C388	P-LCC-68	with mask-programmable ROM, 12 MHz, ext. temperature – 40 to + 85 °C	113
SAB 80C535-N-T40/85	Q 67120-C510	P-LCC-68	for external memory, 12 MHz ext. temperature – 40 to + 85 °C	113
SAB 80C515-16-N	Q 67120-C492	P-LCC-68	with mask-programmable ROM, 16 MHz	113
SAB 80C535-16-N	Q 67120-C509	P-LCC-68	for external memory, 16 MHz	113
SAB 80C535-16-N-T40/85	Q 67120-C562	P-LCC-68	for external memory, 12 MHz ext. temperature – 40 to + 85 °C	113
SAB 80C515A-N18	Q 67120-C581	P-LCC-68	for external memory, 18 MHz	163
SAB 83C515A-5N18	Q 67120-C580	P-LCC-68	with mask-programmable ROM, 18 MHz	163
SAB 80C515A-N18-T3	Q 67120-C784	P-LCC-68	for external memory, 18 MHz ext. temperature – 40 to 85 °C	163

Summary of Types (cont'd)

Type	Ordering Code	Package	Descriptions	Page
SAB 83C515A-5N18-T3	Q 67120-C787	P-LCC-68	with mask-programmable ROM, 18 MHz, ext. temperature – 40 to 85 °C	163
SAB 80C517-N	Q 67120-C397	P-LCC-84	with factory mask-programmable ROM, 12 MHz	221
SAB 80C537-N	Q 67120-C452	P-LCC-84	for external memory, 12 MHz	221
SAB 80C517-N-T40/85	Q 67120-C483	P-LCC-84	with factory mask-programmable ROM, 12 MHz ext. temperature – 40 to 85 °C	221
SAB 80C537-N-T40/85	Q 67120-C484	P-LCC-84	for external ROM, 12 MHz ext. temperature – 40 to 85 °C	221
SAB 80C517 -N16	Q 67120-C723	P-LCC-84	with mask-programmable ROM, 16 MHz	221
SAB 80C537-N16	Q 67120-C722	P-LCC-84	for external memory, 16 MHz	221
SAB 80C517-N16-T40/85	Q 67120-C724	P-LCC-84	with mask-programmable ROM, 16 MHz ext. temperature – 40 to 85 °C	221
SAB 80C537-N16-T40/85	Q 67120-C725	P-LCC-84	for external memory, 16 MHz ext. temperature – 40 to 85 °C	221
SAB 80C517A-N18	Q 67120-C583	P-LCC-84	for external memory, 18 MHz	280
SAB 80C517A-M18	TBD	P-MQFP-100		
SAB 83C517A-5N18	Q 67120-C582	P-LCC-84	with mask-programmable ROM, 18 MHz	280
SAB 80C517A-N18-T3	Q 67120-C769	P-LCC-84	for external memory, 18 MHz ext. temperature – 40 to 85 °C	280
SAB 83C517A-N18-T4	TBD	P-LCC-84	for external memory, 18 MHz ext. temperature – 40 to 110 °C	280
SAB 83C517A-5N18-T3	Q 67120-C771	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature – 40 to 85 °C	280
SAB 803517A-5N18-T4	TBD	P-LCC-84	with factory mask-programmable ROM, 12 MHz ext. temperature – 40 to 110 °C	280
SAB 80C52-N SAB 80C52-P	Q 67120-C396 Q 67120-C379	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz	355

Summary of Types (cont'd)

Type	Ordering Code	Package	Descriptions	Page
SAB 80C32-N SAB 80C32-P	Q 67120-C395 Q 67120-C378	P-LCC-44 P-DIP-40	for external memory, 12 MHz	355
SAB 80C52-P-T40/ 85	Q 67120-C521	P-DIP-40	with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to 85 °C	355
SAB 80C32-P-T40/ 85	Q 67120-C520	P-DIP-40	for external memory, 12 MHz, ext. temperature – 40 to 85 °C	355
SAB 80C52-16-N SAB 80C52-16-P	Q 67120-C503 Q 67120-C501	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 16 MHz	355
SAB 80C32-16-N SAB 80C32-16-P	Q 67120-C502 Q 67120-C500	P-LCC-44 P-DIP-40	for external memory, 16 MHz	355
SAB 80C52-16-P- T40/85	Q 67120-C563	P-DIP-40	with factory mask-programmable ROM, 16 MHz, ext. temperature – 40 to 85 °C	355
SAB 80C32-16-P- T40/85	Q 67120-C527	P-DIP-40	for external memory, 16 MHz, ext. temperature – 40 to 85 °C	355
SAB 80C52-20-N SAB 80C52-20-P	Q 67120-C710 Q 67120-C708	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz	355
SAB 80C32-20-N SAB 80C32-20-P	Q 67120-C711 Q 67120-C709	PL-CC-44 P-DIP-40	for external memory, 20 MHz	355
C500 Derivates				
SAB-C501-LN SAB-C501-LP	Q67120-C844 Q67120-C846	P-LCC-44 P-DIP-40	for external memory , 12 MHz	386
SAB-C501-1RN SAB-C501-1RP	Q67120-C840 Q67120-C842	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz	386
SAB-C501-L20N SAB-C501-L20P	Q67120-C865 Q67120-C866	P-LCC-44 P-DIP-40	for external memory, 20 MHz	386
SAB-C501-1R20N SAB-C501-1R20P	Q67120-C873 Q67120-C874	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz	386
SAB-C501-L40N SAB-C501-L40P	Q67120-C867 Q67120-C868	P-LCC-44 P-DIP-40	for external memory, 40 MHz	386
SAB-C501-1R40N SAB-C501-1R40P	Q67120-C875 Q67120-C876	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 40 MHz	386
SAF-C501-LN SAF-C501-LP	Q67120-C845 Q67120-C847	P-LCC-44 P-DIP-40	for external memory, 12 MHz temp. -40 °C to 85 °C	386
SAF-C501-1RN SAF-C501-1RP	Q67120-C841 Q67120-C843	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz ext. temp. -40 °C to 85 °C	386

Summary of Types (cont'd)

Type	Ordering Code	Package	Descriptions	Page
SAF-C501-L20N SAF-C501-L20P	Q67120-C870 Q67120-C869	P-LCC-44 P-DIP-40	for external memory, 20 MHz temp. -40 °C to 85 °C	386
SAB-C501-1R20N SAB-C501-1R20P	Q67120-C871 Q67120-C872	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz ext. temp. -40 °C to 85 °C	386
SAB-C502-LN SAB-C502-LP	Q67120-C838 Q67120-C889	P-LCC-44 P-DIP-40	for external memory, 12 MHz	427
SAB-C502-2RN SAB-C502-2RP	Q67120-C839 Q67120-C890	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz	427
SAB-C502-L20N SAB-C502-L20P	Q67120-C885 Q67120-C891	P-LCC-44 P-DIP-40	for external memory, 20 MHz	427
SAB-C502-2R20N SAB-C502-2R20P	Q67120-C884 Q67120-C892	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz	427
SAF-C502-LN SAF-C502-LP	Q67120-C883 Q67120-C893	P-LCC-44 P-DIP-40	for external memory, 12 MHz temp. -40 °C to 85 °C	427
SAF-C502-2RN SAF-C502-2RP	Q67120-C886 Q67120-C894	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz ext. temp. -40 °C to 85 °C	427
SAF-C502-L20N SAF-C502-L20P	Q67120-C887 Q67120-C895	P-LCC-44 P-DIP-40	for external memory, 20 MHz temp. -40 °C to 85 °C	427
SAF-C502-2R20N SAF-C502-2R20P	Q67120-C888 Q67120-C896	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz ext. temp. -40 °C to 85 °C	427
SAB-C503-LN	Q67120-C835	P-LCC-44	for external memory, 12 MHz	473
SAB-C503-1RN	Q67120-C834	P-LCC-44	with factory mask-programmable ROM, 12 MHz	473
SAB-C503-L20N	Q67120-C877	P-LCC-44	for external memory, 20 MHz	473
SAB-C503-1R20N	Q67120-C878	P-LCC-44	with factory mask-programmable ROM, 20 MHz	473
SAF-C503-LN	Q67120-C879	P-LCC-44	for external memory, 12 MHz, ext. temp. -40 °C to 85 °C	473
SAF-C503-1RN	Q67120-C880	P-LCC-44	with factory mask-programmable ROM, 12 MHz, ext. temp. -40 °C to 85 °C	473
SAF-C503-L	Q67120-C881	P-LCC-44	for external memory, 20MHz, ext. temp. -40 °C to 85 °C	473

Summary of Types (cont'd)

Type	Ordering Code	Package	Descriptions	Page
SAF-C503-1R20N	Q67120-C882	P-LCC-44	with factory mask-programmable ROM, 20 MHz, ext. temp. -40 °C to 85 °C	473
16-bit Single-Chip Microcontroller				
SAB 80C166-S	Q67120-C493	P-BQFP-100	for external memory, 20 MHz	516
SAB 80C166-M	Q67120-C848	P-MRFP-100		
SAB 83C166-5S	Q67120-C567	P-BQFP-100	with factory mask-programmable ROM, 20 MHz	516
SAB 83C166-5M	Q67120-C849	P-MRFP-100		
SAB 80C166-S-T3	Q67120-C794	P-BQFP-10	for external memory,20 MHz, ext. temp. -40 °C to 85 °C	516
SAB 80C166-M-T3	Q67120-C900	P-MRFP-100		
SAB 83C166-5S-T3	Q67120-C912	P-BQFP-100	with factory mask-programmable ROM, 20 MHz, ext. temp. -40 °C to 85 °C	516
SAB 83C166-5M-T3	Q67120-C911	P-MRFP-100		

8-Bit Single-Chip Microcontrollers

8-Bit Single-Chip Microcontroller — SAB 8051A/8031A Family

Preliminary

SAB 8051A Microcontroller with factory-maskprogrammable ROM
SAB 8031A Microcontroller for external ROM

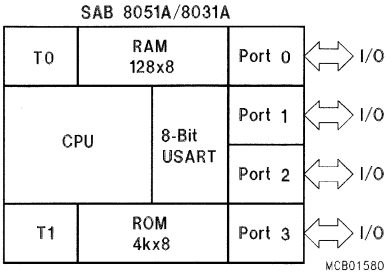
- Version for 12MHz/16MHz/ 20 MHz operating frequency
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive bound rate capability
- External memory expandable up to 128 Kbyte
- Compatible with SAB 8080/8085 peripherals
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  600 ns instruction cycle time at 20 MHz
- 4 µs (3 µs, 2.4 µs) multiply and divide
- Packages P-DIP-40 and P-LCC-44
- Two temperature ranges available
  0 to 70 °C
  –40 to 85 °C : T40/85

The SAB 8051A/8031A Family are standalone, high-performance single-chip microcontrollers fabricated in + 5 V advanced N-channel, silicon-gate Siemens MYMOS technology and supplied in a 40-pin plastic P-DIP or 44-pin plastic leaded chip carrier (P-LCC-44) package. It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full-duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL-compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

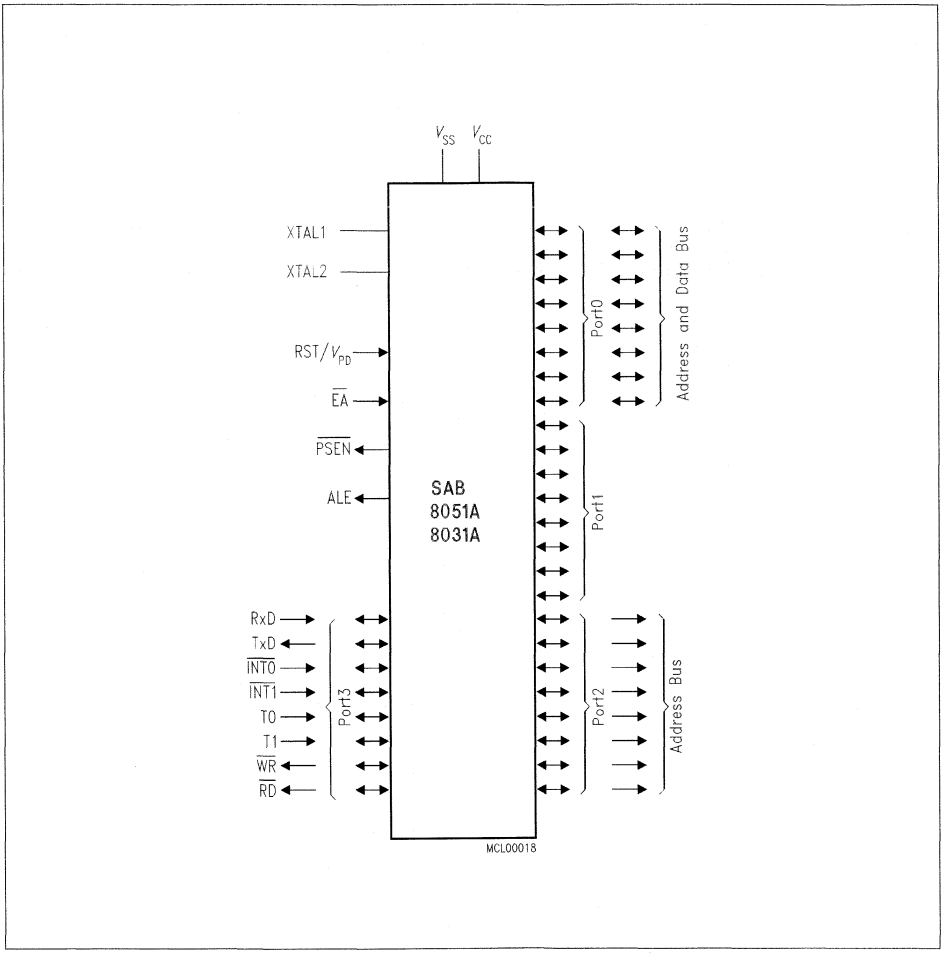
The parts are available for standard temperature range (0 to 70 °C) and extended temperature range (T40/85: – 40 to 85 °C).



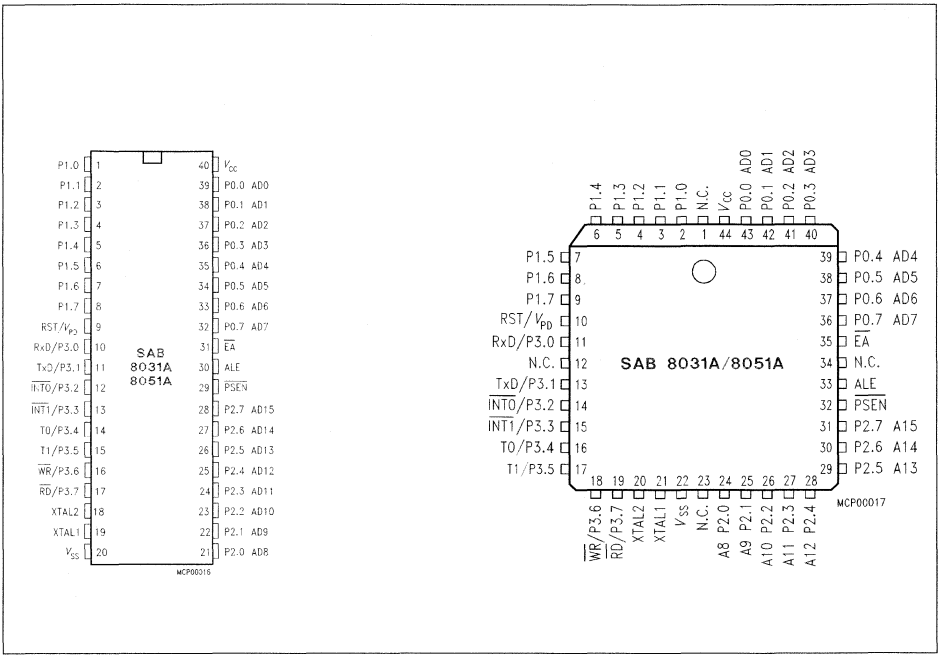
SAB 8051A/8031A Family

Ordering Information

Type	Ordering Code	Package	Description (8-bit single-chip microcontroller)
SAB8031A-P-T40/85	Q 67120-C230	P-DIP-40	for external memory, 12 MHz, ext. Temp.
SAB 8031A-P	Q 67120-C183	P-DIP-40	for external memory,
SAB 8031A-N	Q 67120-C271	P-LCC-44	12 MHz
SAB 8031A-16-P	Q 67120-C347	P-DIP-40	for external memory,
SAB 8031A-16-N	Q 67120-C349	P-LCC-44	16 MHz
SAB 8031A-20-P	Q 67120-C466	P-DIP-40	for external memory,
SAB 8031A-20-N	Q 67120-C467	P-LCC-44	20 MHz
SAB 8051A-P-T40/85	Q 67120-C233	P-DIP-40	with 4-KByte mask-programmable ROM 12 MHz, ext. Temp.
SAB 8051A-P	Q 67120-C186	P-DIP-40	with 4-KByte mask-programmable ROM
SAB 8051A-N	Q 67120-C224	P-LCC-44	12 MHz
SAB 8051A-16-P	Q 67120-C346	P-DIP-40	with 4-KByte mask-programmable ROM
SAB 8051A-16-N	Q 67120-C348	P-LCC-44	16 MHz
SAB 8051A-20-P	Q 67120-C489	P-DIP-40	with 4-KByte mask-programmable ROM
SAB 8051A-20-N	Q 67120-C490	P-LCC-44	20 MHz



Logic Symbol



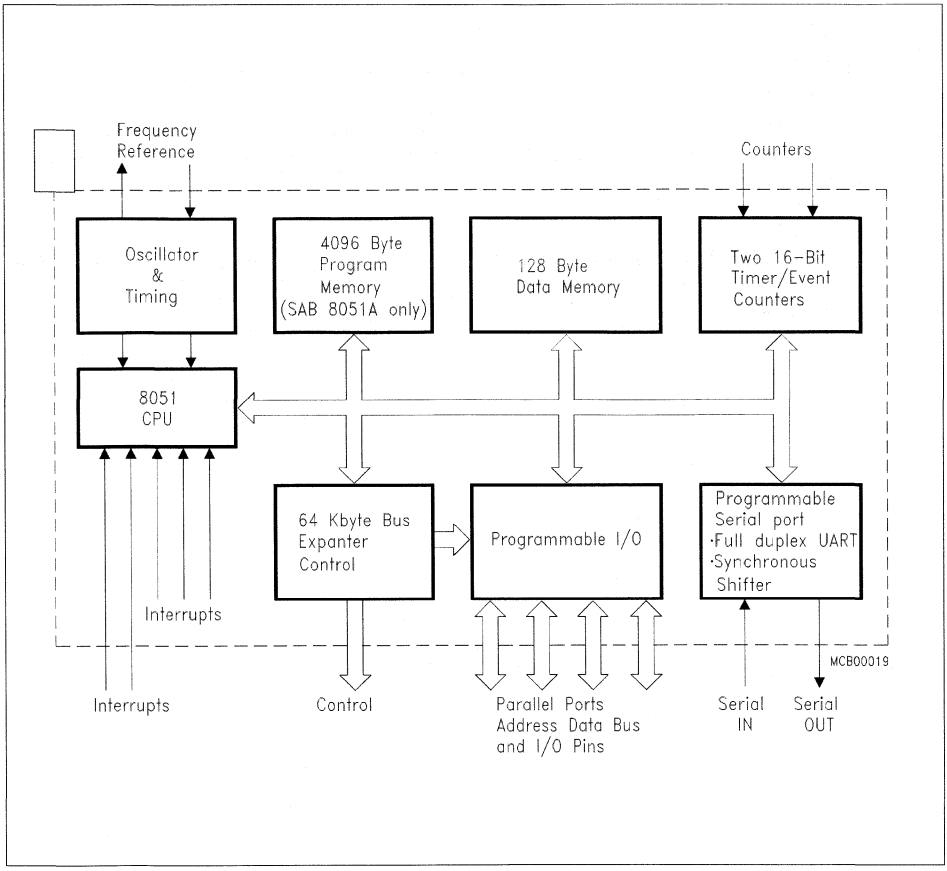
Pin Configuration
P-DIP-40 **P-LCC-44**

Pin Definitions and Functions

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	P-LCC-44		
P1.0-P1.7	1-8	2-9	I/O	**PORT 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/V_{PD}	9	10	I	**RESET** A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	**PORT 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – R_XD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – T_XD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL 1 XTAL 2	19 18	21 20		**XTAL 1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. **XTAL 2** output from the oscillator's amplifier's. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**PORT 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	P-LCC-44		
ALE	30	33	O	Provides **Address Latch Enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	**External Latch Enable** when held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44		+ 5 V **Power Supply** during operation and program verification.
V_{SS}	20	22		**Ground** (0 V)
NC	–	1, 12 23, 34	–	**No Connection**



Block Diagram

Instruction Set

The SAB 8051A/8031A Family has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 8051A/8031A ..... 0 to 70 °C
SAB 8051A/8031A-T40/85 ..... – 40 to 85 °C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 to 7 V
Power dissipation ..... 2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 8051A/8031A
T_A = – 40 to 85 °C for the SAB 8051A/8031A-T40/85

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/VPD and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA

DC Characteristics (cont'd)

Symbol	Parameter	imit Values		Unit	Test Condition
		min.	max.		
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2 SAB 8051A/8031A-12/16/20 SAB 8051A/8031A-T40/85	– –	– 3.2 – 2.5	mA mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} - 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 8051A/8031A SAB 8051A/8031A-16 SAB 8051A/8031A-20 SAB 8051A/8031A-T3	 – – – –	 125 140 140 150	 mA mA mA mA	All outputs disconnected
I_{PD}	Power down current SAB 8051A/8031A-12/16/20 SAB 8051A/8031A-T3	 – –	 10 15	 mA mA	 V_{CC} = 0 V V_{PD} = 4.5 ... 5.5 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for SAB 8051A/8031A, 12 MHz

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C for the SAB 8051A/8031A
T_A = – 40 to 85 °C for the SAB 8051A-T3/8031A-T40/85

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	83.3	833.3	ns
t_{CHCX}	High time	–	–	20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	20	ns
t_{CHCL}	Fall time	–	–	–	20	ns

AC Characteristics for SAB 8051A/8031A, 12 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8051A/8031A-16, 16 MHz

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to + 70 °C for SAB 8051 A/8031A-16

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	33	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	28	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	88	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	48	–	$t_{CLCL}-15$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	60	–	$t_{CLCL}-3$	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}-90$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8051A/8031A-16, 16 MHz(cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	62.5	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

AC Characteristics for SAB 8051A/8031A-20, 20 MHz

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to + 70 °C for SAB 8051A/8031A-20

Symbol	Parameter	Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		Unit
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	60	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	20	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	20	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	100	–	$4t_{CLCL}-100$	ns
t_{LLPL}	$\overline{ALE}$ to $\overline{PSEN}$	25	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	115	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	75	–	$3t_{CLCL}-75$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	47	–	$t_{CLCL}-3$	–	ns
t_{PXIZ}*)	Input instruction float after PSEN	–	40	–	$t_{CLCL}-10$	ns
t_{AVIV}	Address to valid instruction in	–	175	–	$5t_{CLCL}-75$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A-20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

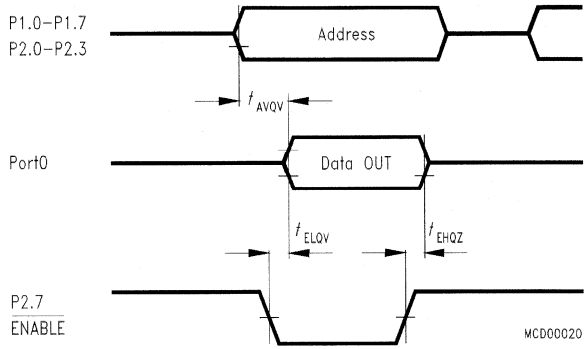
AC Characteristics for SAB 8051A/8031A-20, 20 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
t_{RLRH}	$\overline{RD}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	70	–	$2t_{CLCL}-30$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	100	–	$5t_{CLCL}-150$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	40	–	$2t_{CLCL}-60$	ns
t_{LLDV}	ALE to valid data in	–	250	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	285	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	100	200	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	70	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	20	80	$t_{CLCL}-30$	$t_{CLCL}+30$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5	–	$t_{CLCL}-45$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	200	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	10	–	$t_{CLCL}-40$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns
External Clock Drive						
t_{CLCL}	Oscillator period	–	–	50	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

ROM Verification Characteristics for SAB 8051A/8031A Family

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

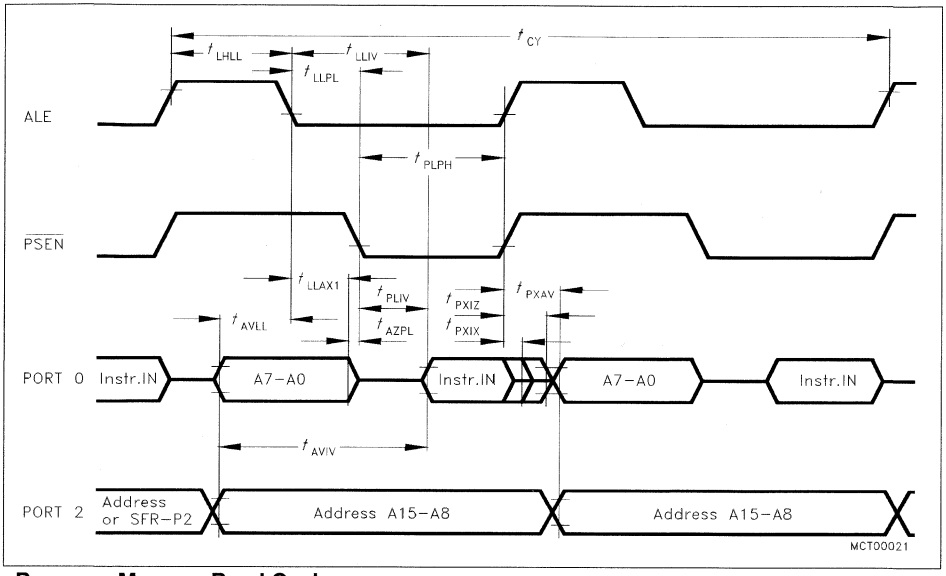
Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz



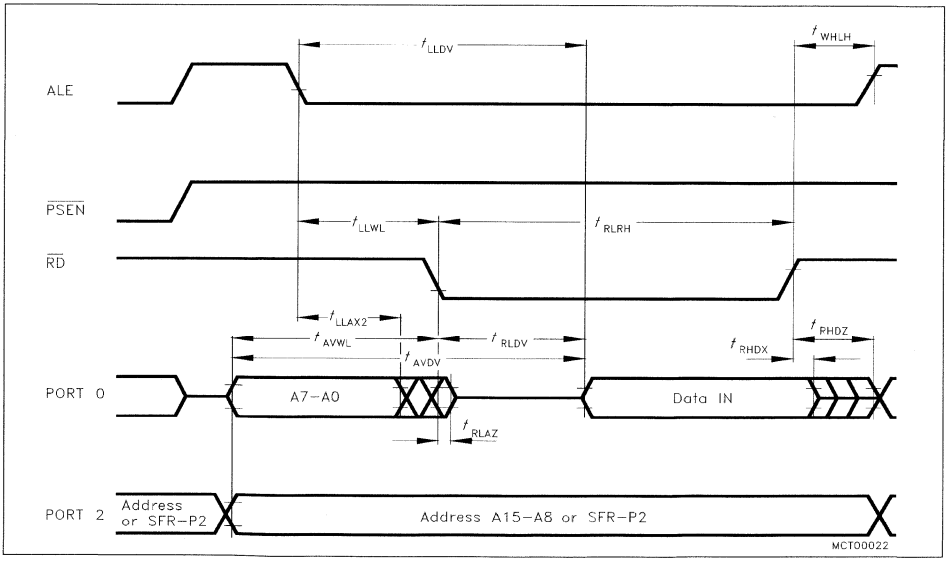
Microcontroller	Address	Data	Inputs
SAB 8051A 4K x 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.3 = A8 – A11	Port 0= D0 – D7	P2.4 – P2.6, PSEN= V_{SS} ALE, EA = V_{IH} R_{ST}/V_{PD} = V_{IH1}

ROM Verification

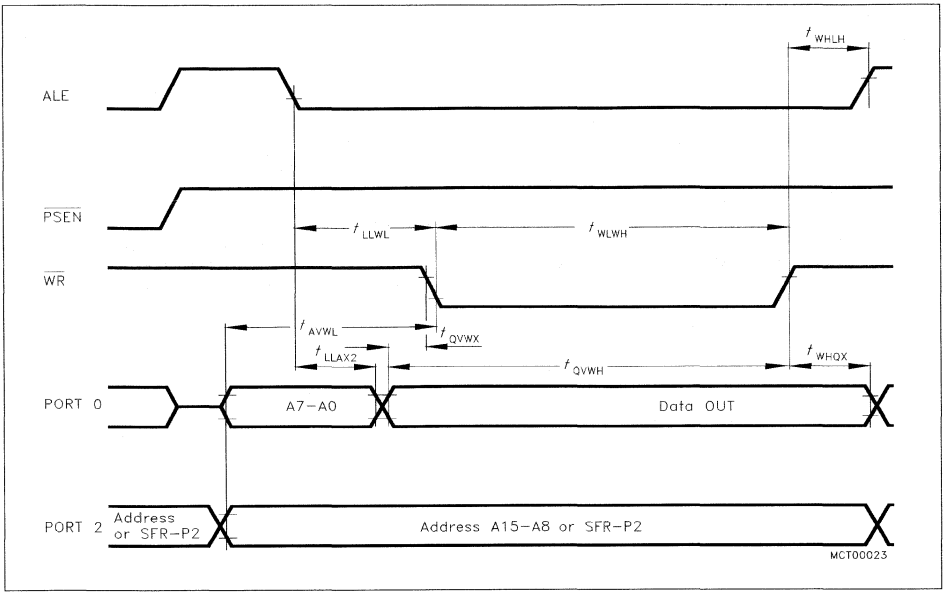
Waveforms



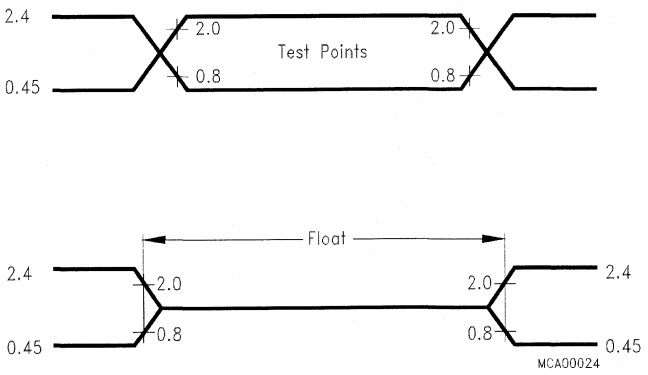
Program Memory Read Cycle



Data Memory Read Cycle

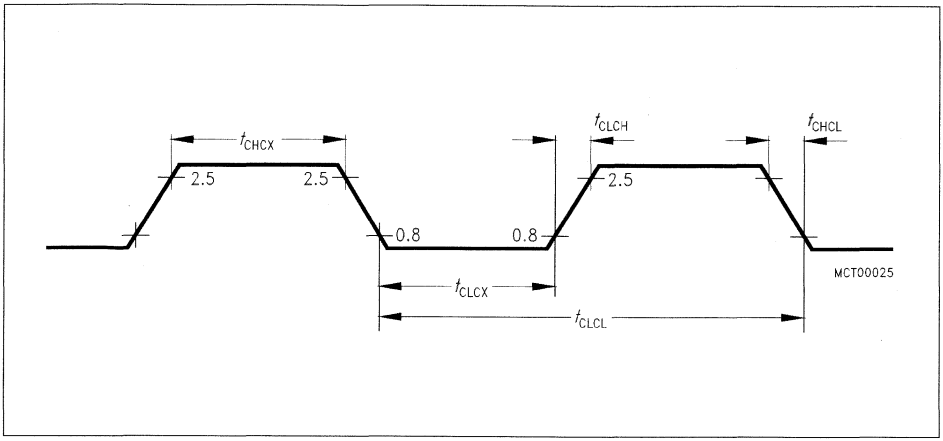


Data Memory Write Cycle

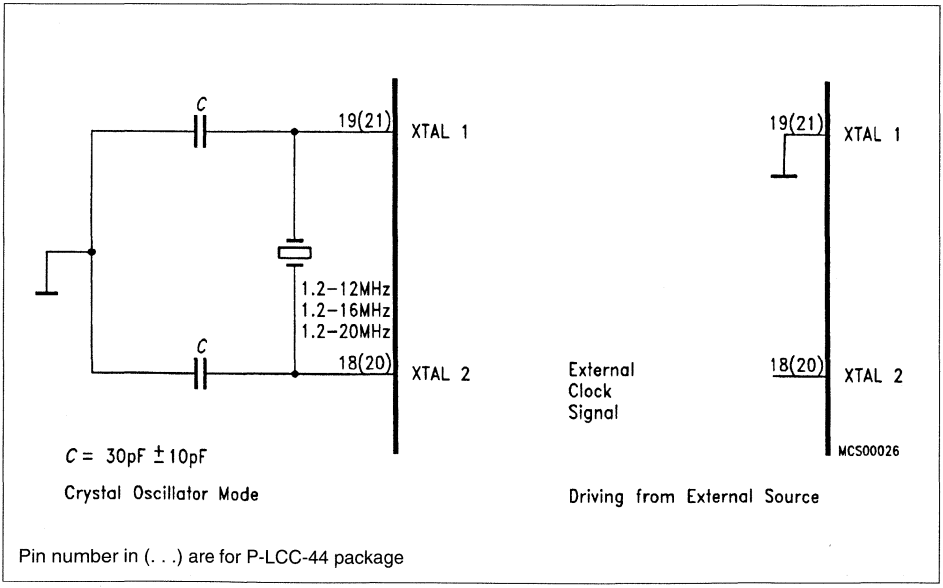


A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

AC Testing Input, Output, Float Waveforms



External Clock Cycle



Recommended Oscillator Circuits

SIEMENS

8-Bit Single-Chip Microcontroller — SAB 8052/8032 Family

Preliminary

SAB 8052B Microcontroller with factory-maskprogrammable ROM (8K)
SAB 80513 Microcontroller with factory mask-programmable ROM (16 K)
SAB 8032B Microcontroller for external ROM

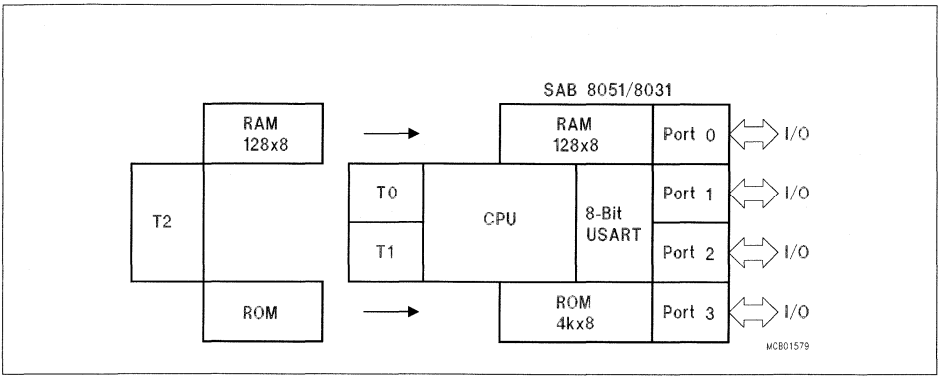
- Versions for 12 MHz / 16 MHz / 20 MHz operating frequency
- 8 K × 8 ROM (SAB 8052B only)
- 16 K × 8 ROM (SAB 80513 only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  600 ns instruction cycle time at 20 MHz
- Multiply and divide in 4 µs/3 µs/2.4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- Packages P-DIP-40 and P-LCC-44
- Full backward compatibility with SAB 8051/8031
- Three temperature ranges available
  0 to 70 °C
  – 40 to 85 °C : T40/85
  – 40 to 110 °C : T40/110

The SAB 8052/8032 family are standalone, high-performance single-chip microcontrollers fabricated in + 5 V advanced N-channel, silicon-gate Siemens MYMOS technology, packaged in a 40-pin plastic dual-in-line package (P-DIP-40) or 44-pin plastic leaded chip carrier (P-LCC-44) package. It is backwardly compatible with the SAB 8051A/8031A and provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The controllers of the SAB 8052 / 8032 family contain a non-volatile 8 K × 8 read-only program memory, SAB 80513 16 K × 8 a volatile 256 × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level nested interrupt structure, a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART, as well as an on-chip oscillator and clock circuits.

For systems that require extra capability, the standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals can be used to expand the SAB 8052 / 8032 family.

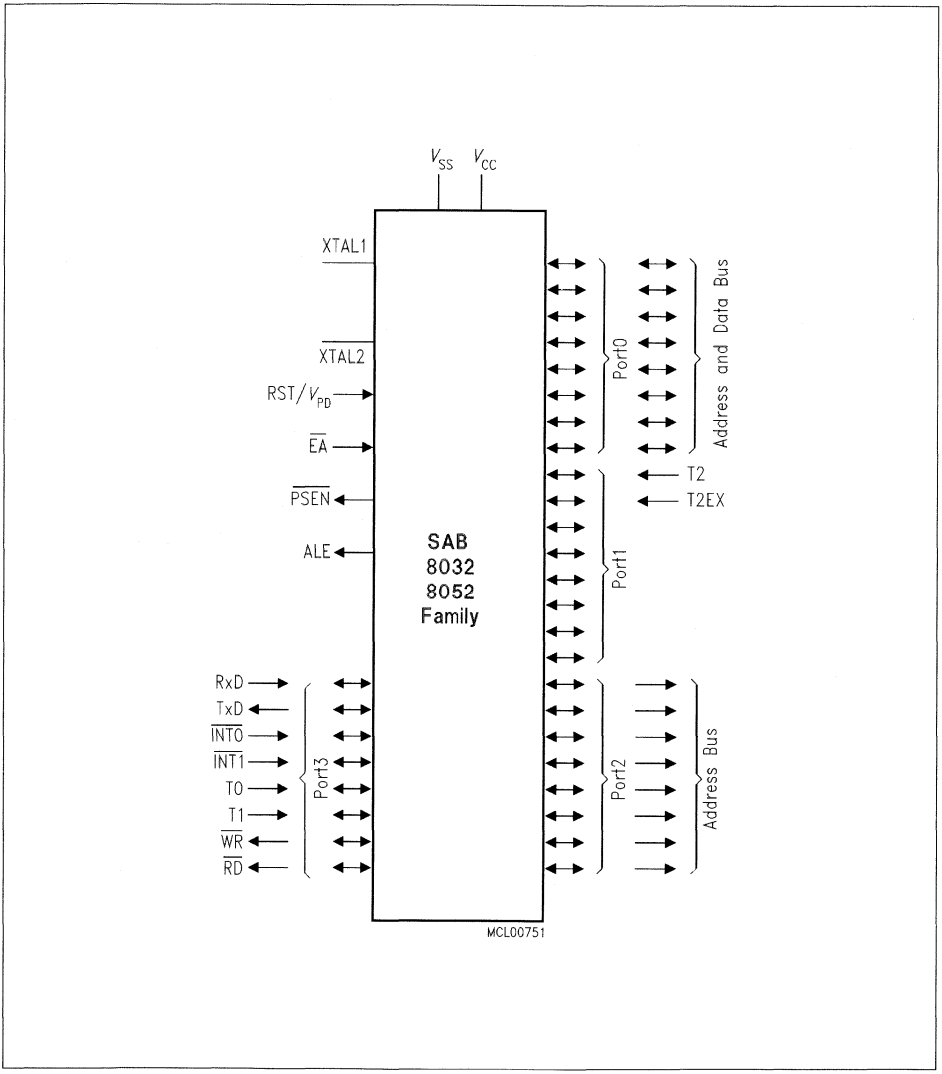
The parts are available for standard temperature range (0 to 70 °C) and extended temperature ranges (T40/85: – 40 to 85 °C and T40/110: – 40 to 110 °C).



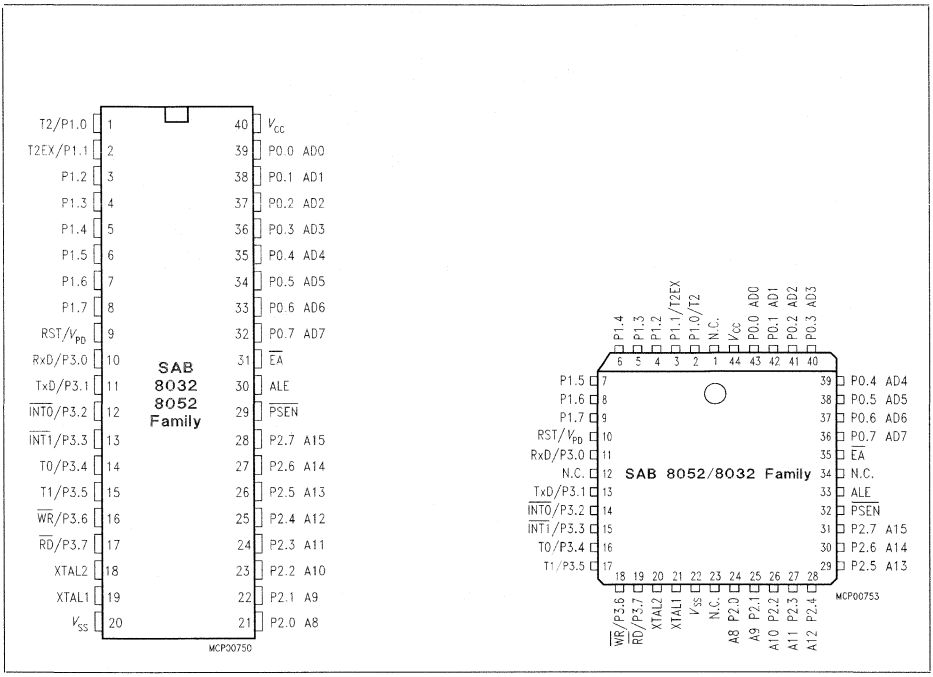
SAB 8052 / 8032 Family

Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 8032B-P	Q 67120-C419	P-DIP-40	for external memory, 12 MHz
SAB 8032B-N	Q 67120-C423		
SAB 8032B-P-T40/85	Q 67120-C427	P-DIP-40	for external memory, 12 MHz ext. Temp.
SAB 8032B-16-P	Q 67120-C421	P-DIP-40	for external memory, 16 MHz
SAB 8032B-16-N	Q 67120-C425	P-LCC-44	
SAB 8032B-20-P	Q 67120-C471	P-DIP-40	for external memory,20 MHz
SAB 8032B-20-N	Q 67120-C472	P-LCC-44	
SAB 8052B-P	Q 67120-C420	P-DIP-40	with 8-KByte mask-programmable ROM, 12 MHz
SAB 8052B-N	Q 67120-C424	P-LCC-44	
SAB 8052B-P-T40/85	Q 67120-C428	P-DIP-40	with 8-KByte mask-programmable ROM, 12 MHz, ext. Temp.
SAB 8052B-16-P	Q 67120-C422	P-DIP-40	with 8-KByte mask-programmable
SAB 8052B-16-N	Q 67120-C426	P-LCC-44	ROM, 16 MHz
SAB 80513-P	Q 67120-C483	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-N	Q 67120-C484	P-LCC-44	ROM, 12 MHz
SAB 80513-16-P	Q 67120-C441	P-DIP-40	with 16-KByte mask-programmable



Logic Symbol



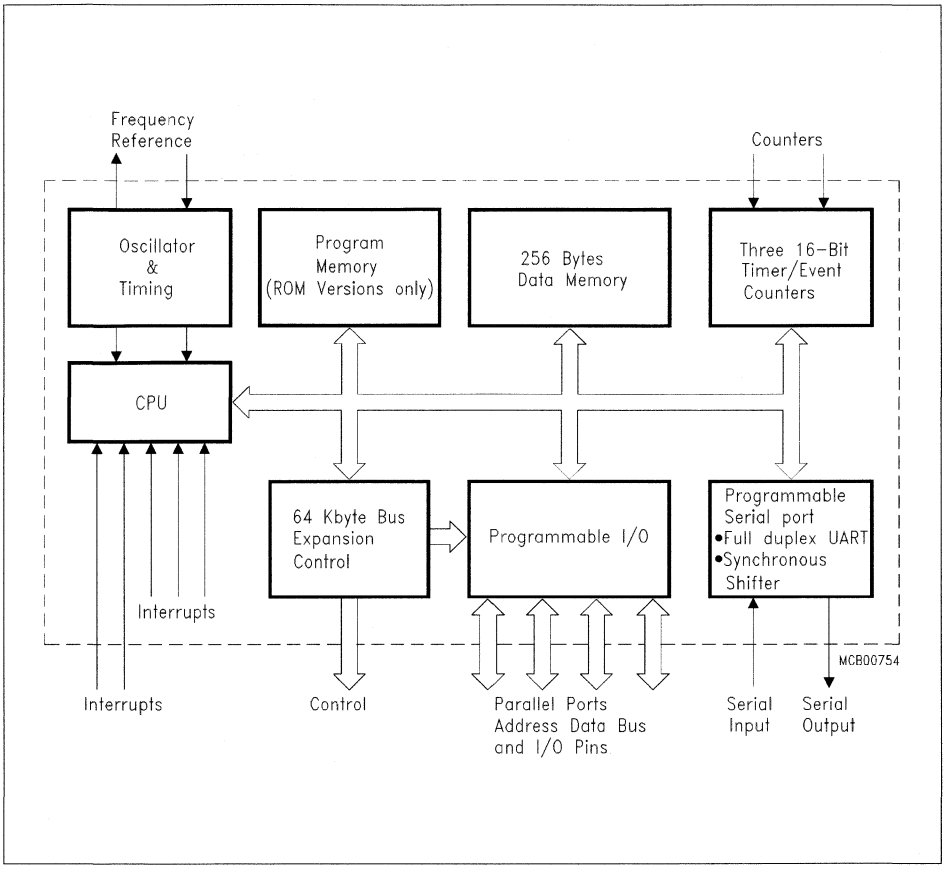
Pin Configuration
P-DIP-40 **P-LCC-44**

Pin Definitions and Functions

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	P-LCC-44		
P1.0-P1.7	1-8	2-9	I/O	**PORT 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 (EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	**RESET** input. A high level on this pin resets the SAB 8052B. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11 13-19	I/O	**PORT 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		**XTAL 1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. **XTAL 2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**PORT 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

Pin Definitions and Functions (continued)

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	P-LCC-44		
$\overline{PSEN}$	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides **Address Latch Enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	**External Access** enable. When held at a TTL high level, the ROM-versions executes instructions from the internal ROM when the PC points to the internal ROM address space. When held at a TTL low level, the ROM-versions fetch all instructions from external program memory. For the ROM-less versions this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+ 5 V **Power Supply** during operation and program verification.
V_{SS}	20	22	–	Circuit **Ground** potential
NC	–	1,12, 23,34	–	**No Connection**



Block Diagram

Instruction Set

The SAB 8052 /8032 Family has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 8052B/8032B/80513 ..... 0 to + 70 °C
SAB 8052B/8032B/80513-T40/85 ..... – 40 to 85 °C
SAB 8032B/80513-T40/110 ..... – 40 to 110 °C
Storage temperature ..... – 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to + 7 V
Power dissipation ..... 2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
T_A = 0 to 70 °C for SAB 8052B/8032B/80513
T_A = – 40 to 85 °C for SAB 8052B/8032B/80513-T40/85
T_A = – 40 to 110 °C for SAB 8032B/80513-T40/110

Symbol	Parameter	Limit Values		Unit	Test Conditions
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test Conditions
		min.	max.		
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2 SAB 8052B/8032B - 12/16/20 SAB 80513 - 12/16 SAB 8052B/8032B - T40/85;T40/110 SAB 80513 - 12/16 - T40/85;T40/110	 – – – –	 – 3.2 – 3.2 – 2.5 – 2.5	 mA mA mA mA mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 8052B/8032B SAB 8052B-16/8032B-16 SAB 8052B-20/8032B-20 SAB 80513 SAB 80513-16 SAB 80513-16-T40/85	 – – – – – –	 175 175 175 175 175 200	 mA mA mA mA mA mA	All outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V; V_{PD} = 4.5 ... 5.5 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

AC Characteristics for SAB 8052B/8032B/80513, 12 MHz

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C for SAB 8052B/8032B/80513
T_A = – 40 to 85 °C for SAB 8052B/8032B/80513-T40/85
T_A = – 40 to 110 °C for SAB 8032B/80513-T40/110

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	83.3	833.3	ns
t_{CHCX}	High time	–	–	20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	20	ns
t_{CHCL}	Fall time	–	–	–	20	ns

AC Characteristics for SAB 8052/8032B/80513, 12 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{\text{PSEN}}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{\text{PSEN}}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{\text{PSEN}}$ to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{\text{PSEN}}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{\text{PSEN}}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{\text{PSEN}}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{\text{PSEN}}$	0	–	0	–	ns

*) Interfacing the SAB 8052B/8032B/80513 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B/8032B/80513, 16 MHz

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C; for SAB 8052B/8032B/80513-16
T_A = – 40 to 85 °C for SAB 80513-16

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	88	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	48	–	t_{CLCL}–15	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	60	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}$–90	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8052B-16/8032B/80513 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B/8032B/80513, 16 MHz(cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	62.5	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

AC Characteristics for SAB 20 MHz/8032B-20, 20 MHz

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	60	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	20	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	20	–	$t_{CLCL}-30$	–	ns
t_{LLIV}	ALE to valid instruction in	–	100	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	25	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	115	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	75	–	$3t_{CLCL}-75$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	40	–	$t_{CLCL}-10$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	47	–	$t_{CLCL}-3$	–	ns
t_{AVIV}	Address to valid instruction in	–	190	–	$5t_{CLCL}-60$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8032B-20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8032B-20, 20 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	200	–	$6t_{CLCL}$ – 100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	200	–	$6t_{CLCL}$ – 100	–	ns
t_{LLAX2}	Address hold after ALE	70	–	$2t_{CLCL}$ – 30	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	100	–	$5t_{CLCL}$ – 150	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	40	–	$2t_{CLCL}$ – 60	ns
t_{LLDV}	ALE to valid data in	–	250	–	$8t_{CLCL}$ – 150	ns
t_{AVDV}	Address to valid data in	–	285	–	$9t_{CLCL}$ – 165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	100	200	$3t_{CLCL}$ – 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	70	–	$4t_{CLCL}$ – 130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	20	80	t_{CLCL} – 30	t_{CLCL} + 30	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5	–	t_{CLCL} – 45	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	200	–	$7t_{CLCL}$ – 150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	10	–	t_{CLCL} – 40	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

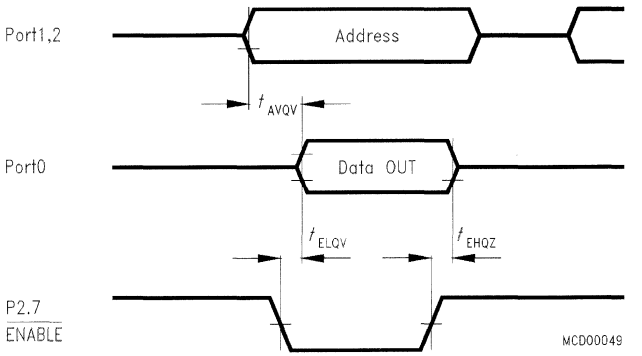
External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	50	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

ROM Verification Characteristics for SAB 8052B/8032B Family

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

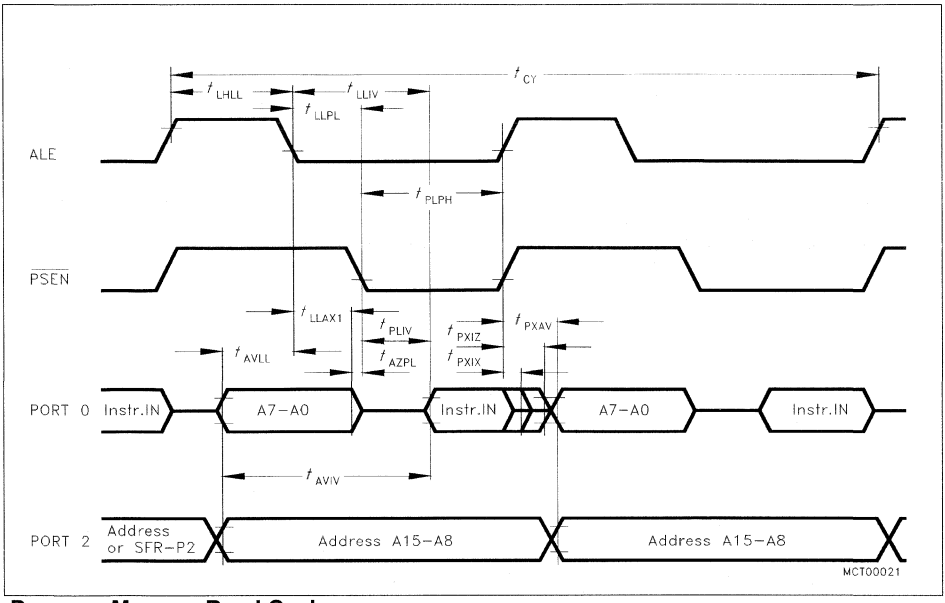
Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz



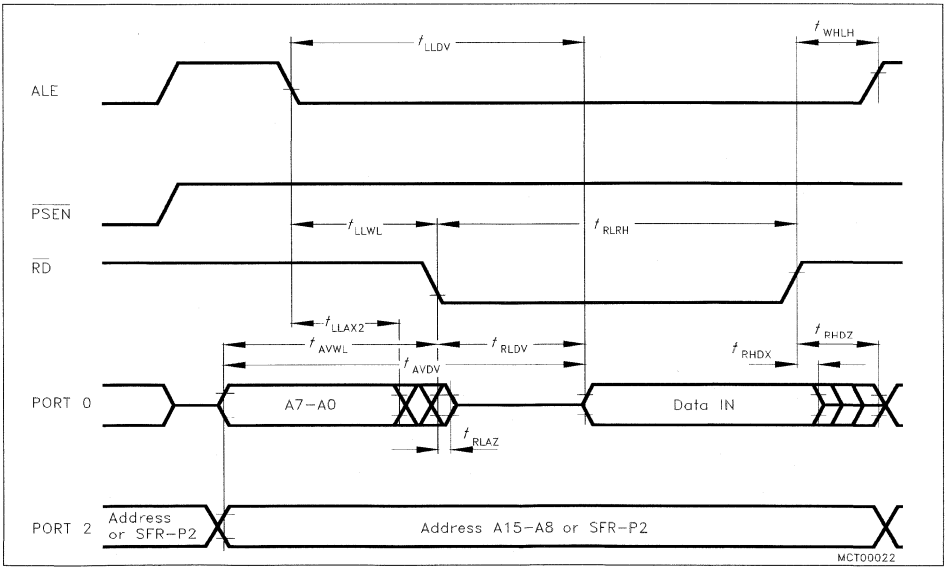
Microcontroller	Address	Data	Inputs	
SAB 8052B 8K × 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.4 = A8 – A12	Port 0 = D0 – D7	P2.5 – P2.6, $\overline{\text{PSEN}}$ ALE, $\overline{\text{EA}}$ R_{ST}/V_{PD}	= V_{SS} = V_{IH} = V_{IH1}
SAB 80513 16K × 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.5 = A8 – A13	Port 0 = D0 – D7	P2.6, $\overline{\text{PSEN}}$ ALE, $\overline{\text{EA}}$ R_{ST}/V_{PD}	= V_{SS} = V_{IH} = V_{IH1}

ROM Verification

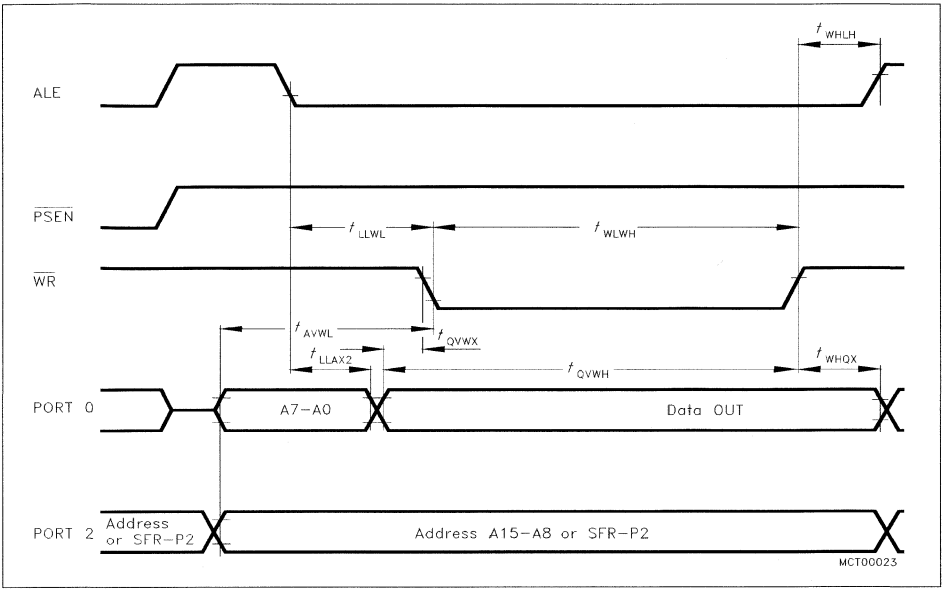
Waveforms



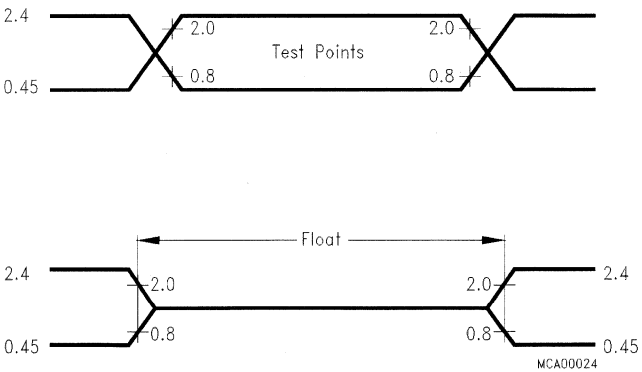
Program Memory Read Cycle



Data Memory Read Cycle

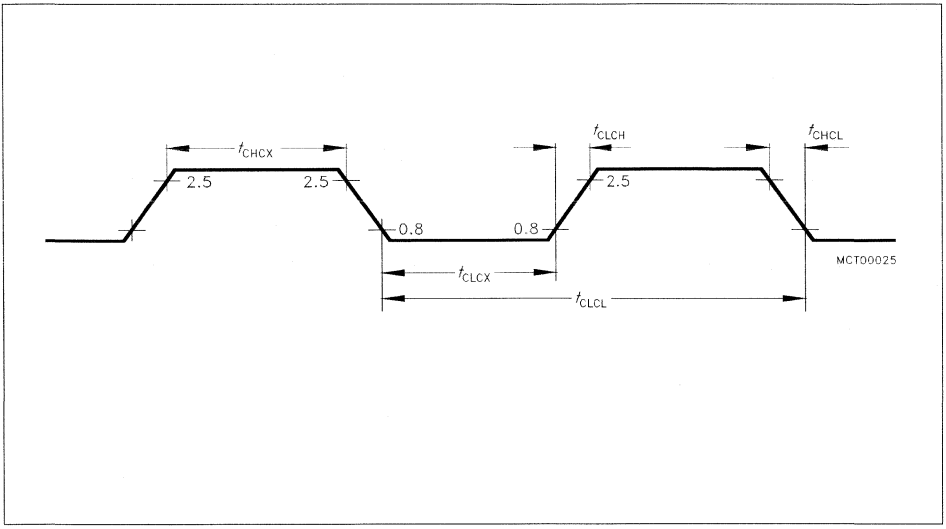


Data Memory Write Cycle

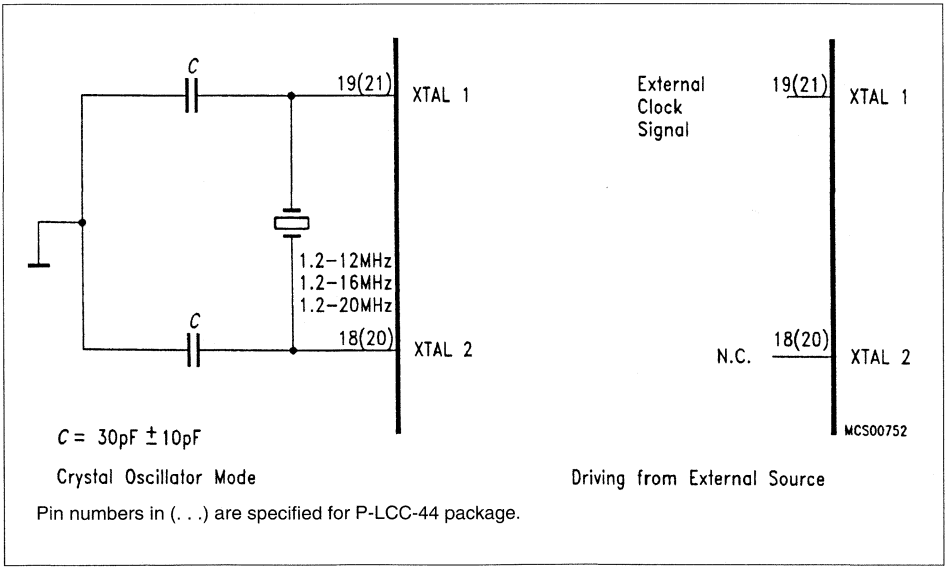


A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

AC Testing Input, Output, Float Waveforms



External Clock Cycle



Recommended Oscillator Circuits

SIEMENS

High-Performance
8-Bit Single Chip Microcontroller

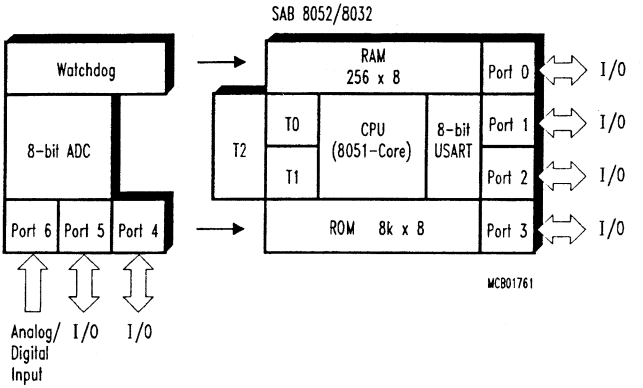
SAB 80515/80535

Preliminary

SAB 80515 Microcontroller with factory mask-programmable ROM
SAB 80535 Microcontroller for external ROM

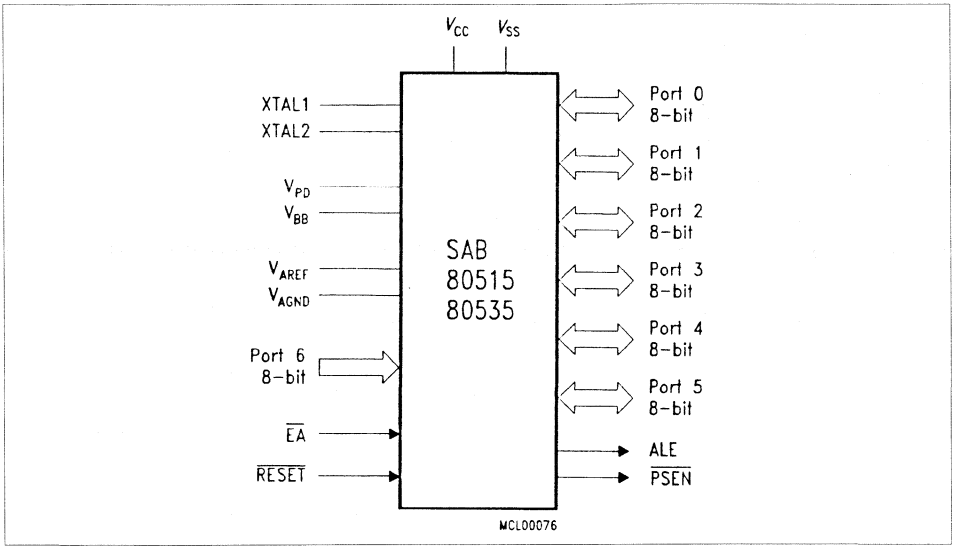
- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processo
- 256-bit-addressable locations
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Three temperature ranges available:
  0 to 70 °C
  – 40 to 85 °C (T40/85)
  – 40 to 110 °C (T40/110)

The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

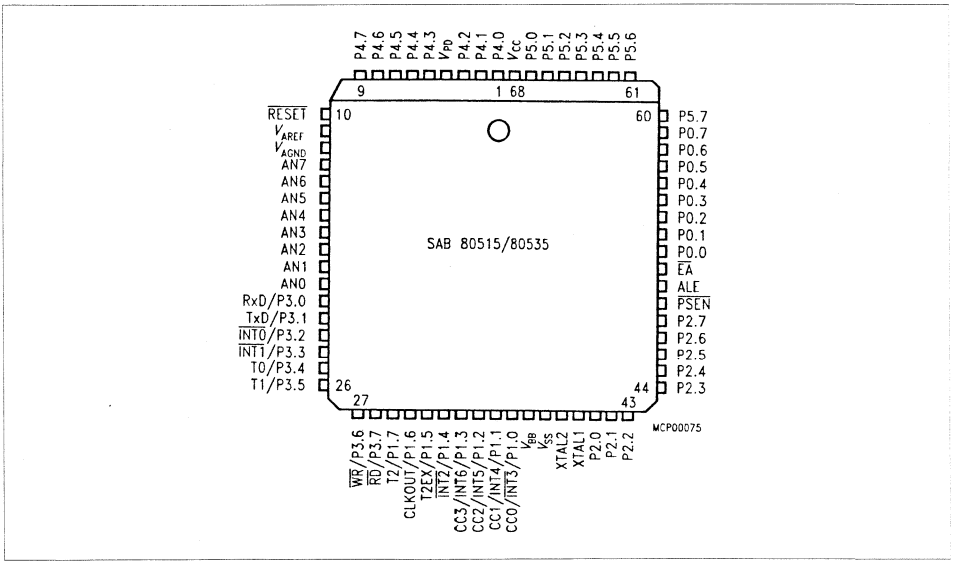


Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80515-N	Q 67120-C211	P-LCC-68	with mask-programmable ROM
SAB 80535-N	Q 67120-C241	P-LCC-68	for external memory
SAB 80515-N-T40/85	Q 67120-C210	P-LCC-68	with mask-programmable ROM
SAB 80535-N-40/85	Q 67120-C240	P-LCC-68	for external memory



Logic Symbol



Pin Configuration
(P-LCC-68)

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port . Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4	I	Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads.The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	Port 1 is an 8-bit bidirectional I/O port .It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{INT2}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39	–	XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40	–	XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0-P2.7	41- 48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{\text{PSEN}}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

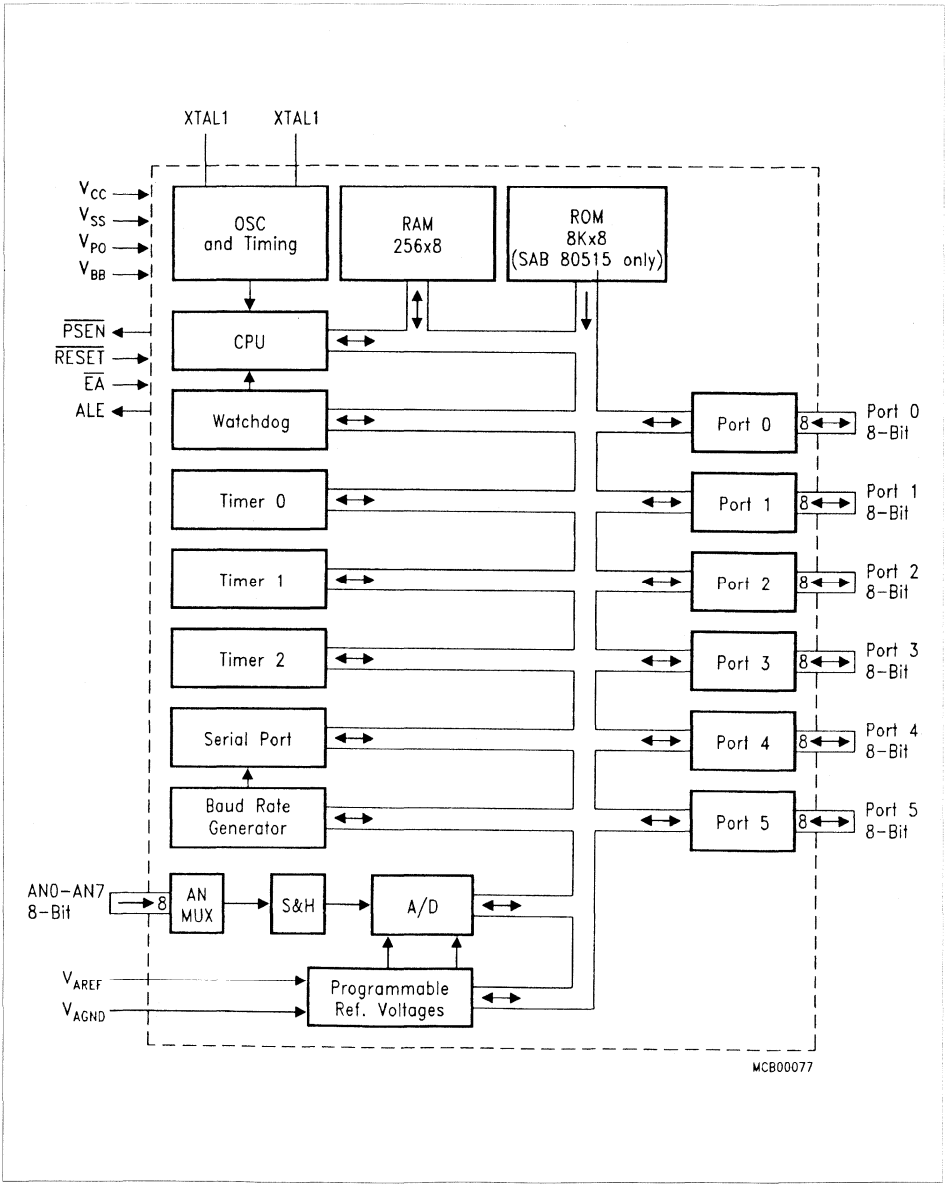


Figure 1
Block Diagram

Functional Description

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described in the following. (Figure 2 illustrates the memory address spaces of the SAB 80515).

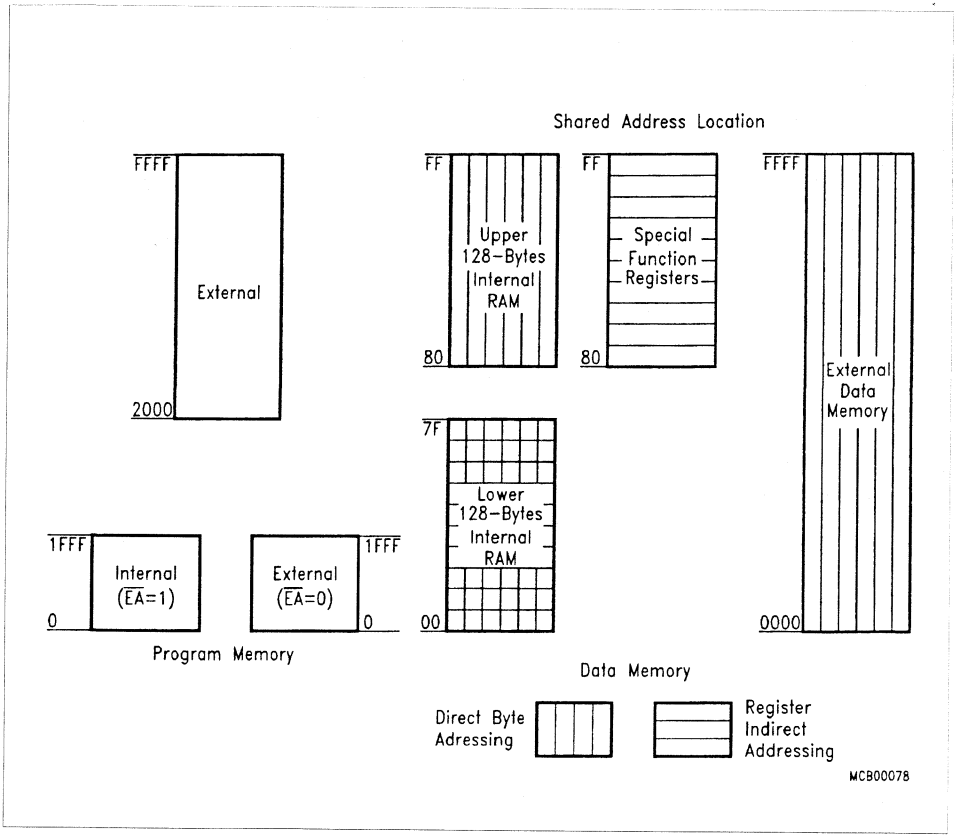


Figure 2
Memory Address Spaces

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

Special Function Registers

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80515/80535.

Table 1
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXXX XXXX B
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	reserved	XXH [2]	9CH	reserved	XXH [2]
85H	reserved	XXH [2]	9DH	reserved	XXH [2]
86H	reserved	XXH [2]	9EH	reserved	XXH [2]
87H	PCON	000X 0000B [2]	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	reserved	XXH [2]	A9H	IP0	X000 0000B [2]
92H	reserved	XXH [2]	AAH	reserved	XXH [2]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3**[1]	**0FFH**	**D0H**	**PSW**[1]	**00H**
B1H	reserved	XXH[2]	D1H	reserved	XXH[2]
B2H	reserved	XXH[2]	D2H	reserved	XXH[2]
B3H	reserved	XXH[2]	D3H	reserved	XXH[2]
B4H	reserved	XXH[2]	D4H	reserved	XXH[2]
B5H	reserved	XXH[2]	D5H	reserved	XXH[2]
B6H	reserved	XXH[2]	D6H	reserved	XXH[2]
B7H	reserved	XXH[2]	D7H	reserved	XXH[2]
B8H	**IEN1**[1]	**00H**	**D8H**	**ADCON**	**00X0 0000 B**[2]
B9H	IP1	XX00 0000B[2]	D9H	ADDAT	00H
BAH	reserved	XXH[2]	DAH	DAPR	00H
BBH	reserved	XXH[2]	DBH	P6	
BCH	reserved	XXH[2]	DCH	reserved	XXH[2]
BDH	reserved	XXH[2]	DDH	reserved	XXH[2]
BEH	reserved	XXH[2]	DEH	reserved	XXH[2]
BFH	reserved	XXH[2]	DFH	reserved	XXH[2]
C0H	**IRCON**[1]	**00H**	**E0H**	**ACC**[1]	**00H**
C1H	CCEN	00H	E1H	reserved	XXH[2]
C2H	CCL1	00H	E2H	reserved	XXH[2]
C3H	CCH1	00H	E3H	reserved	XXH[2]
C4H	CCL2	00H	E4H	reserved	XXH[2]
C5H	CCH2	00H	E5H	reserved	XXH[2]
C6H	CCL3	00H	E6H	reserved	XXH[2]
C7H	CCH3	00H	E7H	reserved	XXH[2]
C8H	**T2CON**[1]	**00H**	**E8H**	**P4**[1]	**0FFH**
C9H	reserved	XXH[2]	E9H	reserved	XXH[2]
CAH	CRCL	00H	EAH	reserved	XXH[2]
CBH	CRCH	00H	EBH	reserved	XXH[2]
CCH	TL2	00H	ECH	reserved	XXH[2]
CDH	TH2	00H	EDH	reserved	XXH[2]
CEH	reserved	XXH[2]	EEH	reserved	XXH[2]
CFH	reserved	XXH[2]	EFH	reserved	XXH[2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B**[1]	**00H**	**F8H**	**P5** [1]	**0FFH**
F1H	reserved	XXH[2]	F9H	reserved	XXH[2]
F2H	reserved	XXH[2]	FAH	reserved	XXH[2]
F3H	reserved	XXH[2]	FBH	reserved	XXH[2]
F4H	reserved	XXH[2]	FCH	reserved	XXH[2]
F5H	reserved	XXH[2]	FDH	reserved	XXH[2]
F6H	reserved	XXH[2]	FEH	reserved	XXH[2]
F7H	reserved	XXH[2]	FFH	reserved	XXH[2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumululator	**0E0H** [1]	00H
	B	B-Register	**0F0H** [1]	00H
	DPH	Data Pointer, High Byte	083H	00H
	DPL	Data Pointer, Low Byte	082H	00H
	PSW	Program Status Word Register	**0D0H** [1]	00H
	SP	Stack Pointer	081H	07H
A/D-Converter	ADCON [2]	A/D Converter Control Register	**0D8H** [1]	00X0 0000 B [3]
	ADDAT	A/D Converter Data Register	09DH	00H
	DAPR	A/D Converter Program Register	0DAH	00H)
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1 [2]	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0 [2]	Interrupt Priority Register 0	0A9H	X000 0000 B [3]
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000 B [3]
	IRCON	Interrupt Request Control Register	**0C0H** [1]	00H
	TCON [2]	Timer Control Register	**88H** [1]	00H
	T2CON [2]	Timer 2 Control Register	**0C8H** [1]	00H
Compare/ Capture- Unit Compare/ Capture- Unit (CCU) (cont'd) (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2. Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON [2]	Timer 2 Control Register [1]	**0C8H** [1]	00H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks
3) X means that the value is indeterminate

Table 2
Special Function Registers- Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80H** [1]	0FFH
	P1	Port 1	**90H** [1]	0FFH
	P2	Port 2	**0A0H** [1]	0FFH
	P3	Port 3	**0B0H** [1]	0FFH
	P4	Port 4	**0E8H** [1]	0FFH
	P5	Port 5	**0F8H** [1]	0FFH
	P6	Port 6, Analog/Digital Input	0DBH	
Pow. Sav. Modes	PCON [2]	Power Control Register	087H	000X 0000 B [2]
Serial Channels	ADCON [2]	A/D Converter Control Reg.	**0D8H** [1]	00X0 0000 B [3]
	PCON [2]	Power Control Register	087H	000X 0000 B [3]
	SBUF	Serial Channel Buffer Reg.	099H	XXXX XXXX B [3]
	SCON	Serial Channel Control Reg.	**098H** [1]	00H
Timer 0/ Timer 1	TCON [2]	Timer Control Register	**088H** [1]	00H
	TH0	Timer 0. High Byte	08CH	00H
	TH1	Timer 1, High Byte	08DH	00H
	TL0	Timer 0, Low Byte	08AH	00H
	TL1	Timer 1, Low Byte	08BH	00H
	TMOD	TImer Mode Register	089H	00H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1 [2]	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0 [2]	Interrupt Priority Register 0	0A9H	X000 0000 B [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 3 shows a block diagram of the A/D converter.

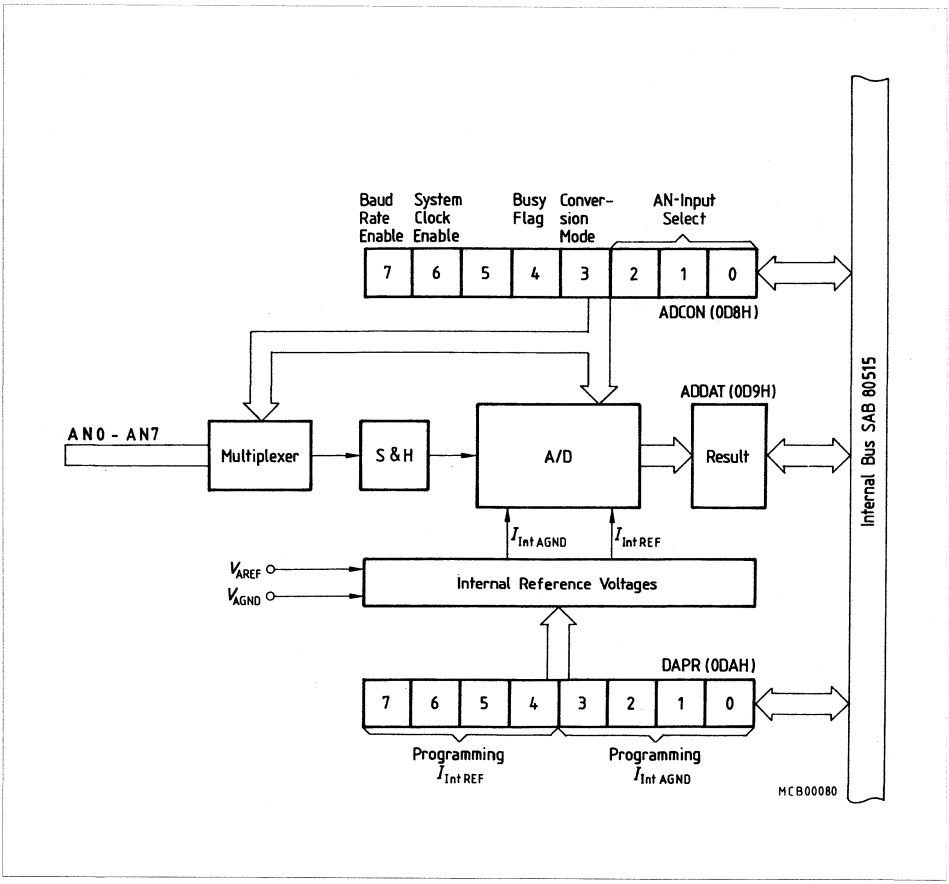


Figure 3
Block Diagram of the A/D Converter

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 4 shows a block diagram of the timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

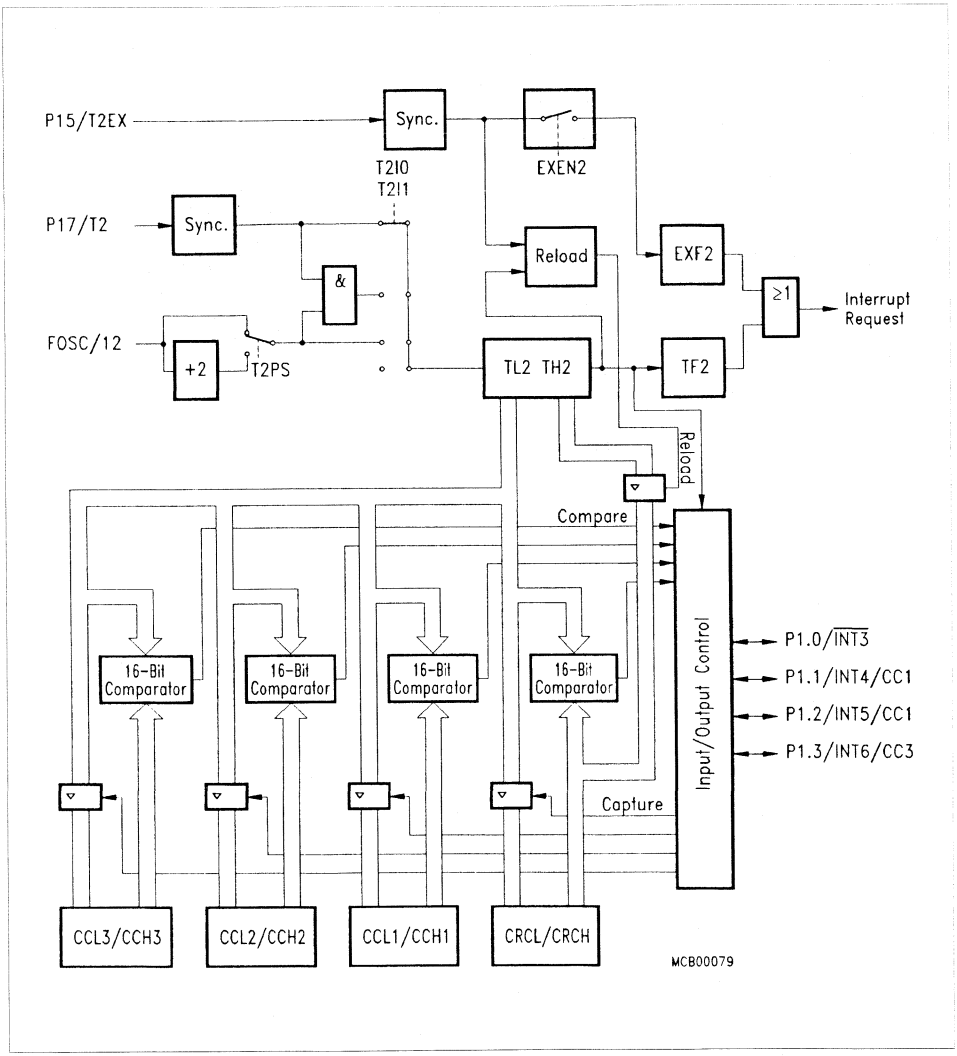


Figure 4
Block Diagram of Timer/Counter 2

Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 3
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 interrupt
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 interrupt
RI + TI	0023H	Serial port interrupt
TF2 + EXF2	002BH	Timer 2 interrupt
IADC	0043H	A/D converter interrupt
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

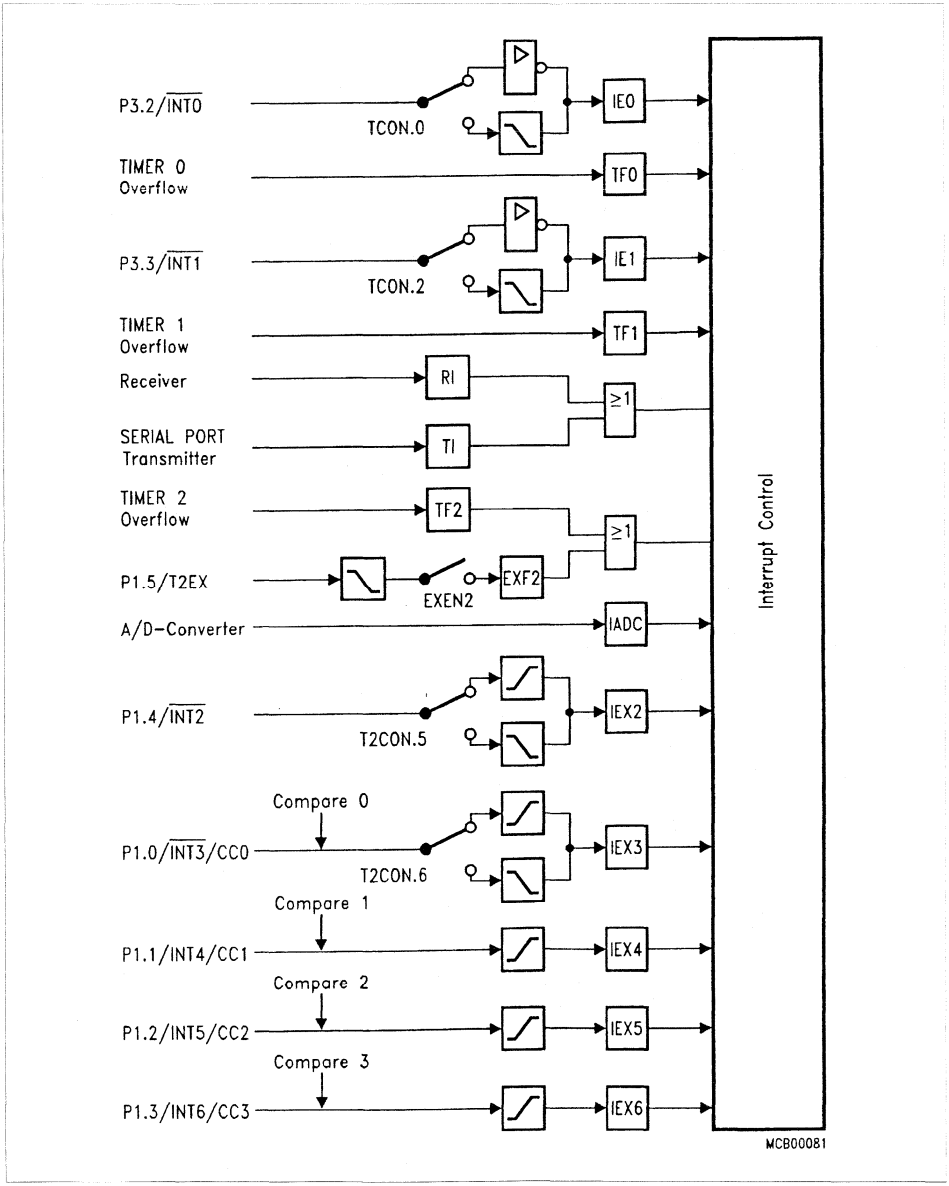


Figure 5
Interrupt Request Sources

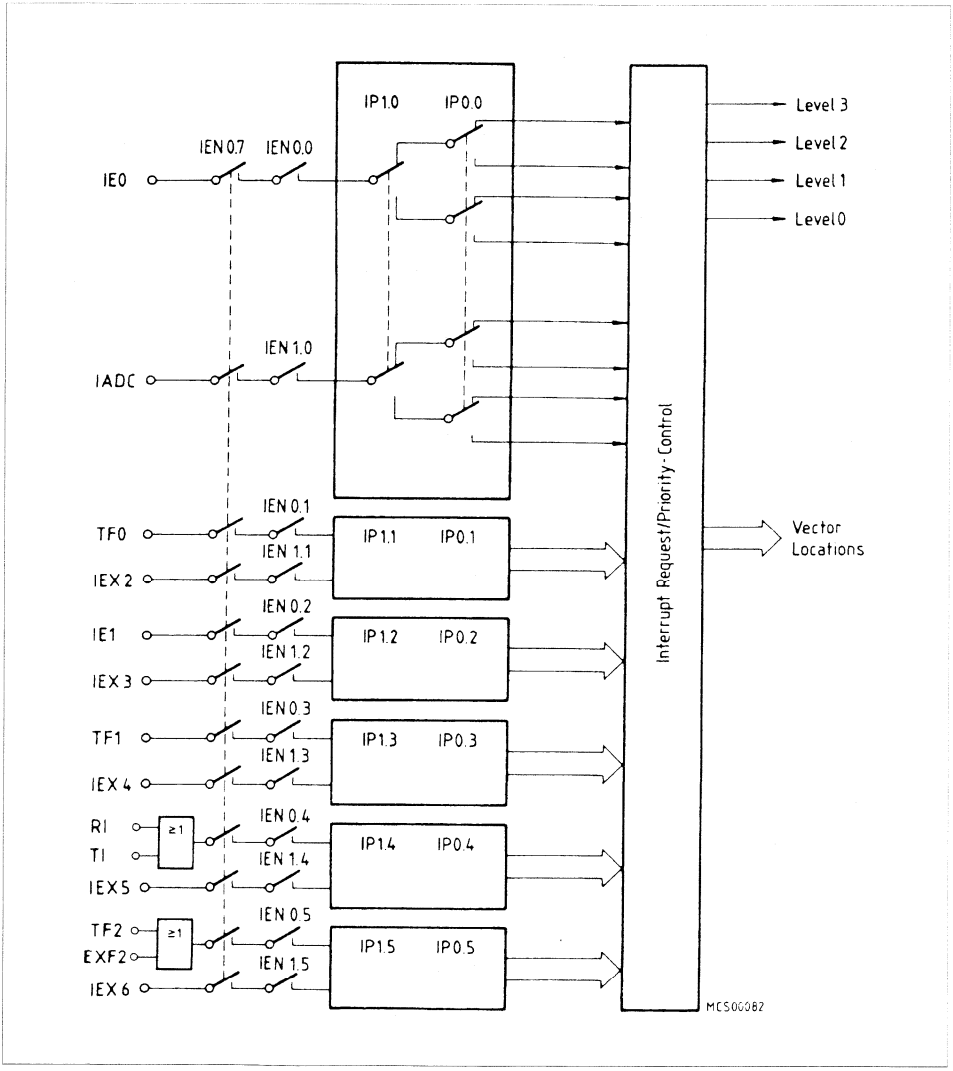


Figure 6
Priority Level Structure

I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

The SAB 80515/80535 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-B6599 - X - X - 7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80515/80535 ..... 0 to 70 °C
SAB 80515/80535-T40/85 ..... – 40 to 85 °C
SAB 80515/80535-T40/110 ..... – 40 to 110 °C
Storage temperature ..... – 65 to 150 °C
Voltage on any pins with respect to ground (V_{SS}) ..... – 0.5 V to 7 V
Power dissipation ..... 2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80515/80535
T_A = – 40 to 85 °C for the SAB 80515/80535-T40/85
T_A = – 40 to110 °C for the SAB 80515/80535-T40/110

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage) (except $\overline{\text{RESET}}$, XTAL2	V_{IH}	2.0	V_{CC} – 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	2.5	V_{CC}+ 0.5	V	XTAL1 to V_{SS}
Input high voltage to $\overline{\text{RESET}}$	V_{IH2}	3.0	–	V	–
Power down voltage	V_{PD}	3	5.5	V	V_{CC} = 0 V
Output low voltage ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1)]
Output low voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OL1}	–	0.45	V	I_{OL}= 3.2mA [1)]
Output high voltage ports 1, 2, 3, 4, 5	V_{OH}	2.4	–	V	I_{OH}= –80 µA
Output high voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OH1}	2.4	–	V	I_{OH}= –400 µA

[1)] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Logic 0 input current ports 1, 2, 3, 4, 5	I_{IL}	–	– 800	µA	V_{IL} = 0.45 V
Logic 0 input current XTAL2	I_{IL2}	–	– 2.5	mA	XTAL1=V_{SS} V_{IL} = 0.45 V
Input low current to $\overline{\text{RESET}}$ for reset	I_{IL3}	–	–500	µA	V_{IL} = 0.45 V
Input leakage current to port 0, $\overline{\text{EA}}$ AN0 - AN7	I_{LI}	–	± 10	µA	0 V< V_{IN} < V_{CC}
Power supply current:[1]					
SAB 80515/80535	I_{CC}	–	210	mA	all outputs
SAB 80515/80535-T40/85	I_{CC}	–	230	mA	disconnected
SAB 80515/80535-T40/110	I_{CC}	–	230	mA	
Power-down current	I_{PD}	–	3	mA	V_{CC} = 0 V
Capacitance of I/O buffer	C_{IO}	–	10	pF	f_C=1 MHz

[1] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to +70 °C for SAB 80515/80535
T_A = -40 to +85 °C for SAB 80515/80535 - T40/85
T_A = -40 to +110 °C for SAB 80515/80535 - T40/110

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}- 0.2	–	V_{AREF}+ 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	1)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	5 t_{CY}	µs	–
Conversion time (including sample time)	t_C	–	–	15 t_{CY}	µs	–
Differential non-linearity Integral non-linearity Offset error Gain error Total unadjusted error	DNLE INLE TUE	–	± 1/2 ± 1/2 ± 1/2 ± 1/2 ± 1	± 1 ± 1 ± 1 ± 1 ± 2	LSB LSB LSB LSB LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 2)
V_{AREF} supply current	I_{REF}	–	–	5	mA	2)
Internal reference error	$V_{IntREFER}$	–	± 5	± 15	mV	2)

1) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I)during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

A/D Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; (C_L for port 0, ALE and PSEN outputs = 100 pF;
C_L for all other outputs = 80 pF) T_A = 0 to + 70 °C; for SAB 80515/80535
T_A = -40 to + 85 °C; for SAB 80515/80535 - 40/85
T_A = -40 to + 110 °C; for SAB 80515/80535 - 40/110

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	

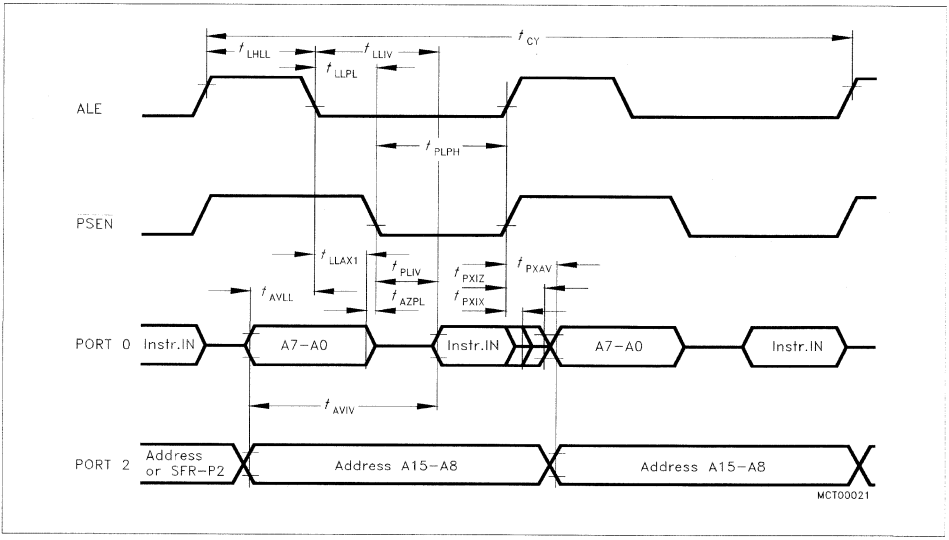
Program Memory Characteristics

Cycle Time	t_{CY}	1000	–	12 t_{CLCL}	–	ns
ALE pulse width	t_{LHLL}	127	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX1}	48	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	4 t_{CLCL} – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215		3 t_{CLCL} – 35	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	150	–	3 t_{CLCL} –100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	t_{CLCL} - 8	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	5 t_{CLCL} – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

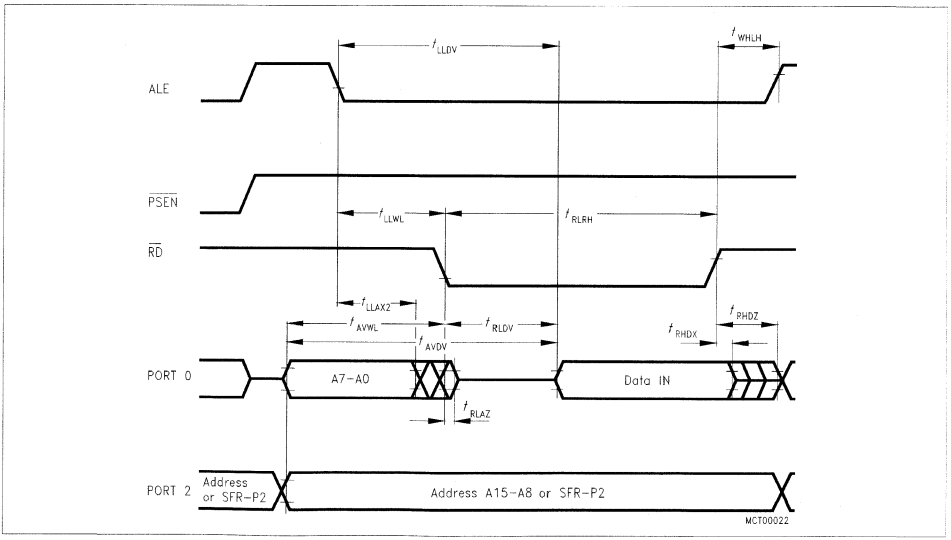
*) Interfacing the SAB 805156 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6\,t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6\,t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2\,t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5\,t_{CLCL} - 165$	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2\,t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8\,t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9\,t_{nCLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3\,t_{CLCL} - 50$	$3\,t_{CLCL} + 50$	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4\,t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7\,t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

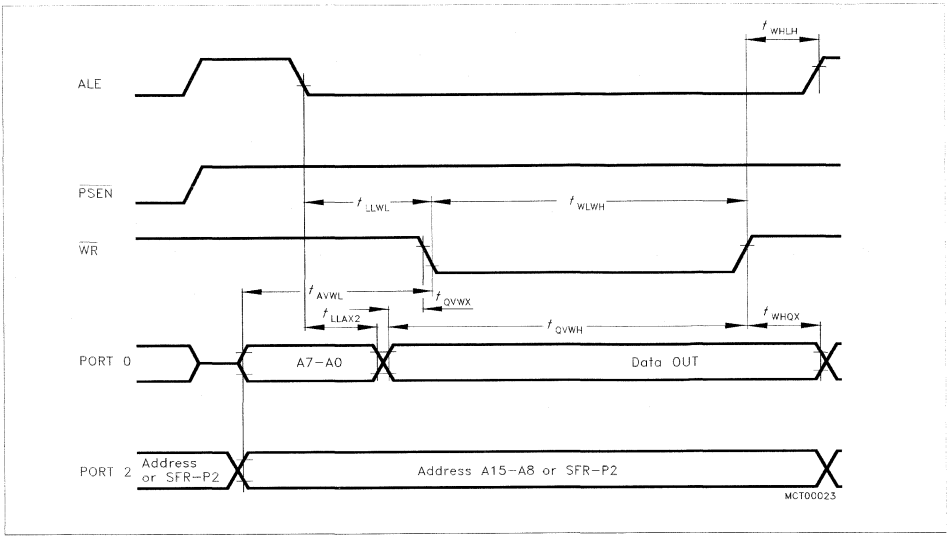
Waveforms



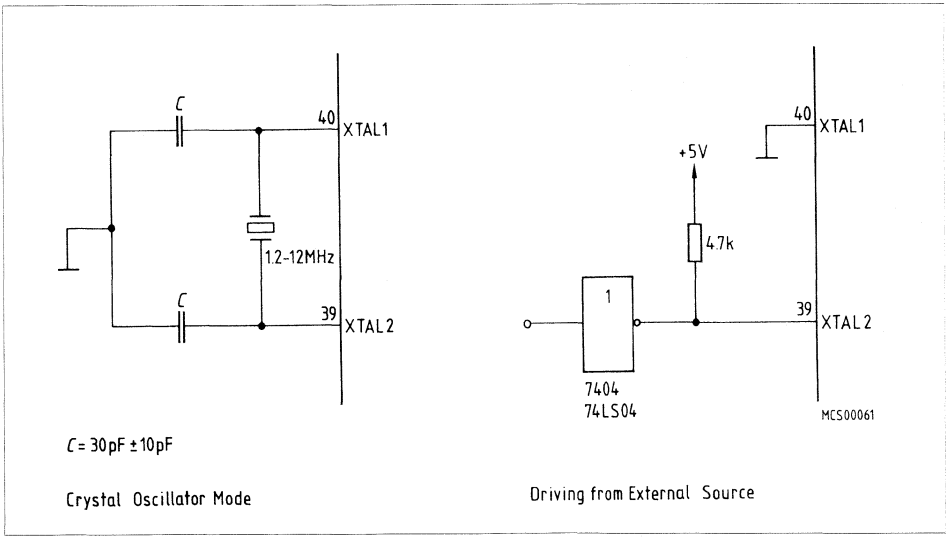
Program Memory Read Cycle



Data Memory Read Cycle



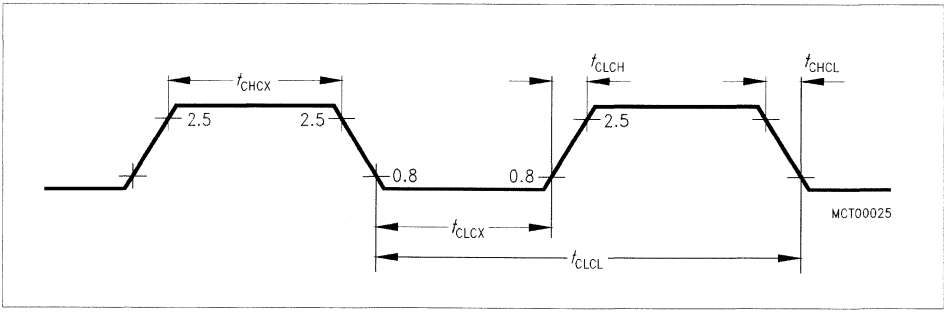
Data Memory Write Cycle



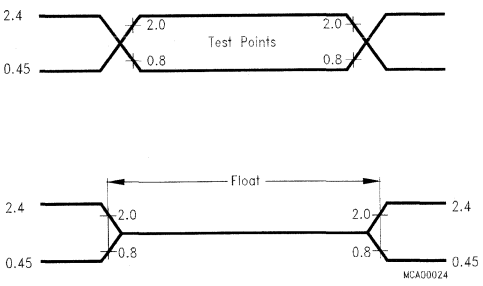
Recommended Oscillator Circuits

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1.2 MHz to 12 MHz		
		min.	max.	
External Clock Drive XTAL2				
Oscillator period	t_{CLCL}	83.3	833.3	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator period	t_{CLCL}	83.3	833.3	ns



External Clock Cycle

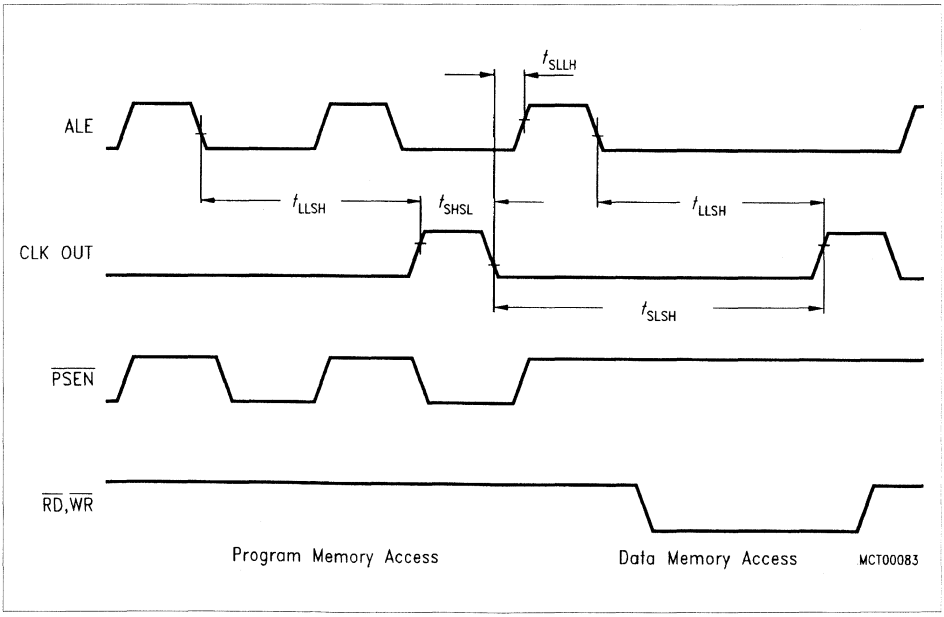


A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

A.C. Testing Input, Output, Float Waveforms

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



System Clock Timing

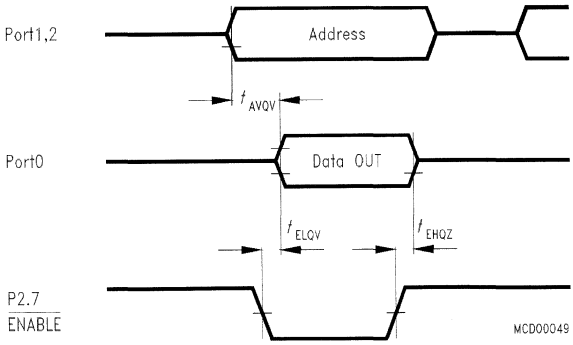
ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	

ROM Verification

Address to valid data	t_{AVQV}	–	48 t_{CLCL1}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL1}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL1}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

Data: Port 0 = D0-D7

Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

ROM Verification

SIEMENS

High-Performance
8-Bit CMOS Single-Chip Microcontroller

SAB 80C515/80C535

Preliminary

SAB 80C515/80C515-16 CMOS microcontroller with factory mask-programmable ROM
SAB 80C535/80C535-16 CMOS microcontroller for external ROM

- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one input port for digital or analog input
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- Boolean processor
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Functionally compatible with SAB 80515
- Idle and power-down mode
- Plastic leaded chip carrier package: P-LCC-68
- Three temperature ranges available:
  0 to 70 °C (for 12 NHz)
  – 40 to 85 °C (for 12/16 MHz)
  – 40 to 110 °C (for 12 MHz)

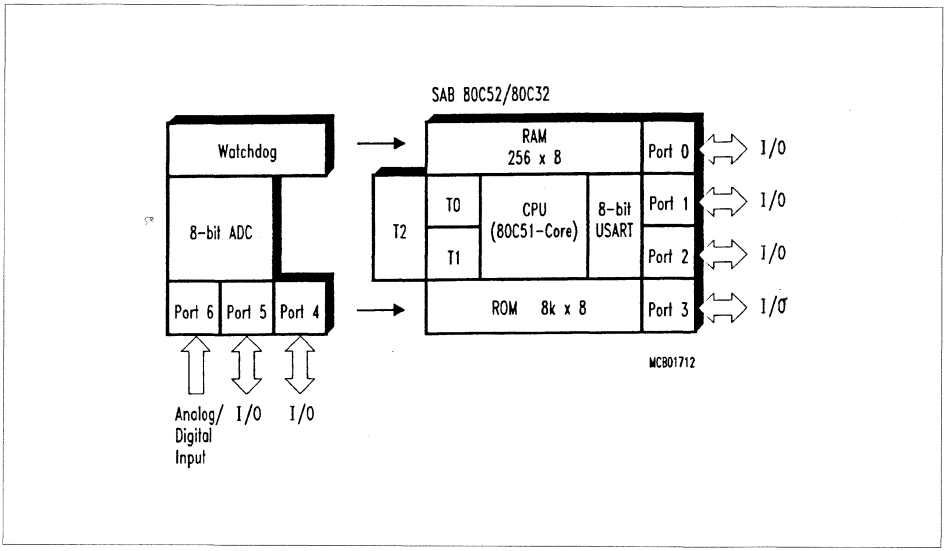
The SAB 80C515/80C535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is designed in Siemens ACMOS technology and is functionally compatible with the SAB 80515/80535 devices designed in MYMOS technology.

The SAB 80C515/80C535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051/80C51 architecture. While maintaining all the SAB 80C51 operating characteristics, the SAB 80C515/80C535 incorporates several enhancements which significantly increase design flexibility and overall system performance.

In addition, the low-power properties of Siemens ACMOS technology allow applications where power consumption and dissipation are critical. Furthermore, the SAB 80C515/80C535 has two software-selectable modes of reduced activity for further power reduction: idle and power-down mode.

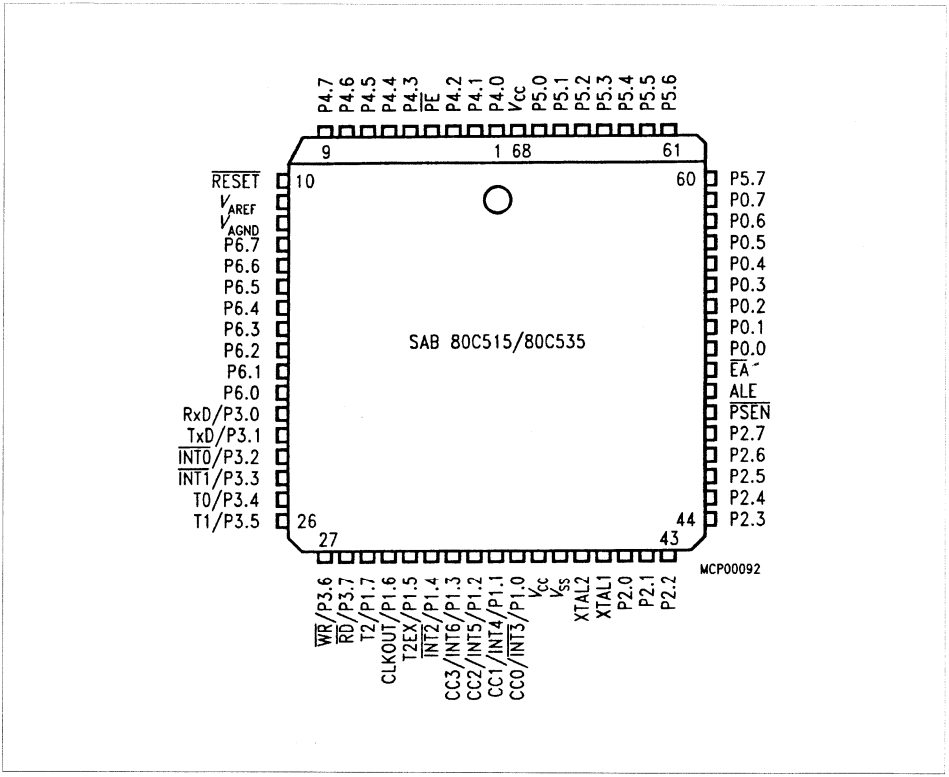
The SAB 80C535 is identical with the SAB 80C515 except that it lacks the on-chip program memory. The SAB 80C515/80C535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

There are versions for 12 MHz operation and for 16 MHz operation and for extended temperature ranges -40 to 85°C and -40 to 110 °C available.

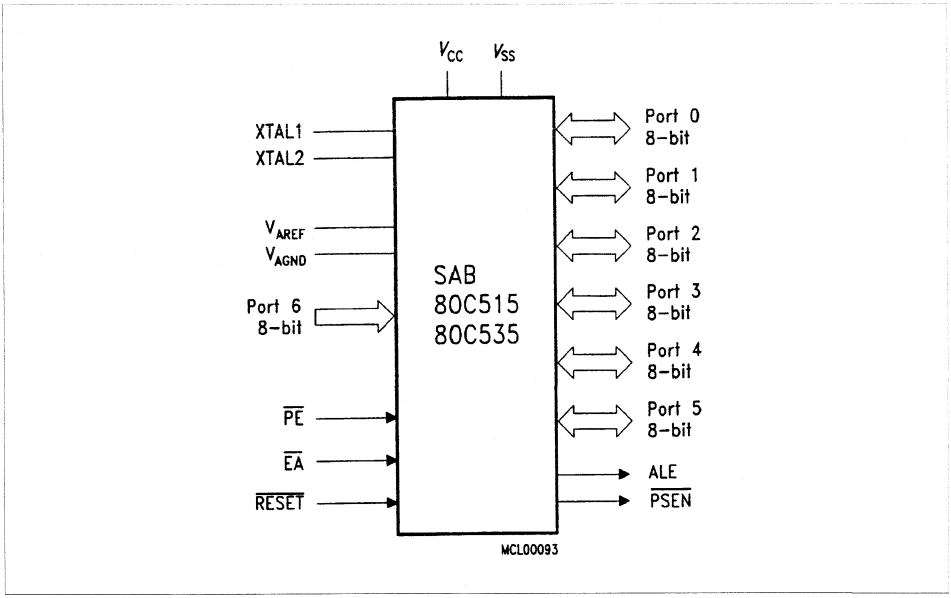

SAB 80C52/80C32
Watchdog
8-bit ADC
Port 6
Port 5
Port 4
Analog/ Digital Input
I/O
I/O
RAM 256 x 8
T2
T0
T1
CPU (80C51-Core)
8-bit USART
ROM 8k x 8
Port 0
Port 1
Port 2
Port 3
I/O
I/O
I/O
I/O
MCB01712

Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C515-N	Q 67120-C297	P-LCC-68	with mask-programmable ROM, 12 MHz
SAB 80C535-N	Q 67120-C508	P-LCC-68	for external memory, 12 MHz
SAB 80C515-N-T40/85	Q 67120-C388	P-LCC-68	with mask-programmable ROM, 12 MHz ext. temperature – 40 to + 85 °C
SAB 80C535-N-T40/85	Q 67120-C510	P-LCC-68	for external memory, 12 MHz ext. temperature – 40 to + 85 °C
SAB 80C515-16-N	Q 67120-C492	P-LCC-68	with mask-programmable ROM, 16 MHz
SAB 80C535-16-N	Q 67120-C509	P-LCC-68	for external memory, 16 MHz
SAB 80C535-16-N-T40/85	Q 67120-C562	P-LCC-68	for external memory, 16 MHz ext. temperature – 40 to + 85 °C



Pin Configuration
(P-LCC-68)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	P-LCC-68	**Port 4** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
$\overline{PE}$	4	I	**$\overline{Power\ saving\ mode\ enable}$** A low level on this pin enables the use of the power saving modes (idle mode and power-down mode). When $\overline{PE}$ is held on high level it is impossible to enter the power saving modes.
$\overline{RESET}$	10	I	**$\overline{Reset\ pin}$** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		**Reference voltage** for the A/D converter
V_{AGND}	12		**Reference ground** for the A/D converter
P6.7-P6.0	13-20		**Port 6** is an 8-bit undirectional input port. Port pins can be used for digital input if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs of the A/D converter.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P3.0-P3.7	21-28	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input/ compare 0 output/capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/ compare **1** output/capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/ compare 2 output/capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/ compare 3 output/capture 3 input – $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
XTAL2 XTAL1	39 49		**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	41- 48	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	O	The **Program store enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	O	The **Address latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{EA}$	51	I	**External access enable** When held high, the SAB 80C515 executes instructions from the internal ROM as long as the PC is less than 8192. When held low, the SAB 80C515 fetches all instructions from external program memory. For the SAB 80C535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
V_{CC}	37		**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 68.
V_{SS}	38		**Ground** (0 V)
V_{CC}	68		**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 37.

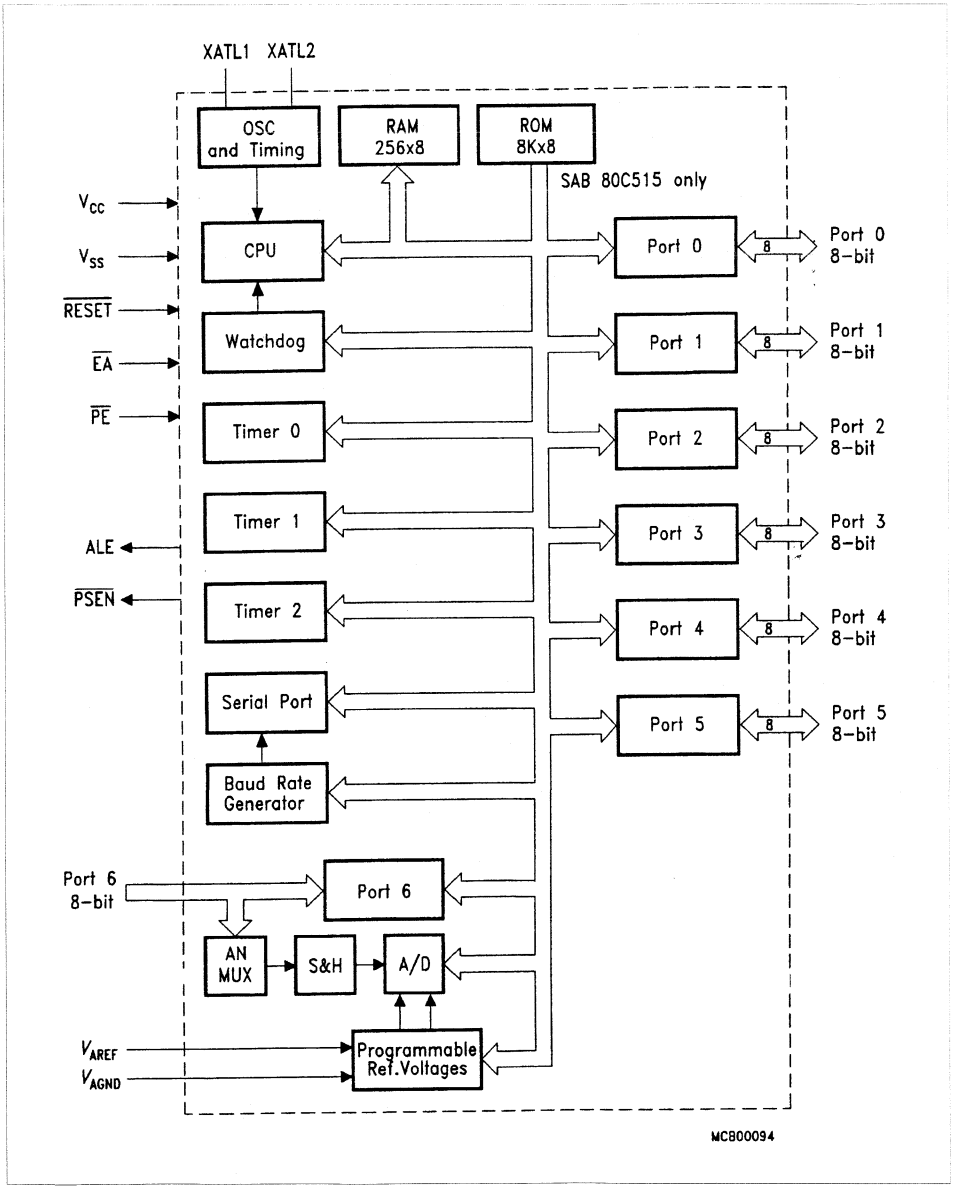


Figure 1
Block Diagram

Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515

The SAB 80C535 is identical to the SAB 80C515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80C515" is used to refer to both the SAB 80C515 and SAB 80C535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80C515 is based on the SAB 8051/SAB 80C51 microcontroller family. The following features of the SAB 80C515 are fully compatible with the SAB 80C51 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80C515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on-chip.
The SAB 80C515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains at 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog or digital signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80C515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80C515.

CPU

The SAB 80C515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80C515 manipulates operands in the four memory address spaces described below: Figure 1 illustrates the memory address spaces of the SAB 80C515.

Program Memory

The SAB 80C515 has 8 Kbyte of on-chip ROM, while the SAB 80C535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80C515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held now, the SAB 80C515 fetches all instructions from the external program memory. Since the SAB 80C535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks:
the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 byte special function register (SRF) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes. The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

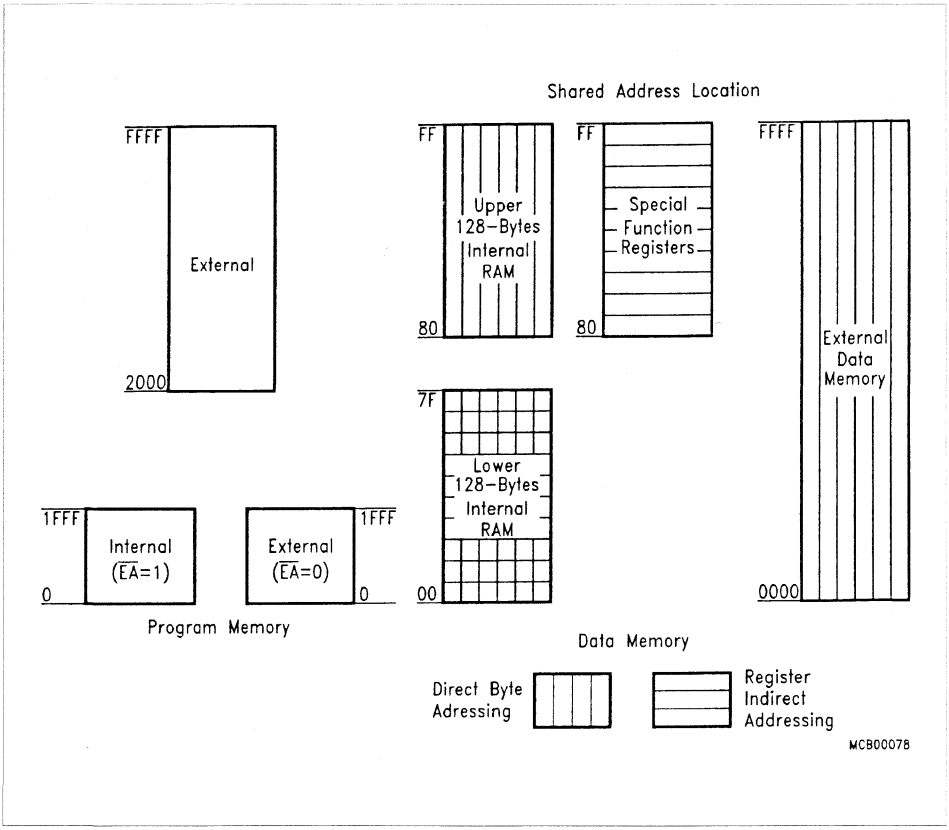


Figure 2
Memory Address Spaces

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 1 and table 2.

In table 1 they are organized in numeric order of their addresses. In table 3 they are organized in groups which refer to the functional blocks of the SAB 80C515.

Table 1: Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXH [2]
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	reserved	XXH [2]	9CH	reserved	XXH [2]
85H	reserved	XXH [2]	9DH	reserved	XXH [2]
86H	reserved	XXH [2]	9EH	reserved	XXH [2]
87H	PCON	00H	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	reserved	XXH [2]	A9H	IP0	00H
92H	reserved	XXH [2]	AAH	reserved	XXH [2]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1:Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3**[1]	**0FFH**	**D0H**	**PSW**[1]	**00H**
B1H	reserved	XXH[2]	D1H	reserved	XXH[2]
B2H	reserved	XXH[2]	D2	reserved	XXH[2]
B3H	reserved	XXH[2]	D3H	reserved	XXH[2]
B4H	reserved	XXH[2]	D4H	reserved	XXH[2]
B5H	reserved	XXH[2]	D5H	reserved	XXH[2]
B6H	reserved	XXH[2]	D6H	reserved	XXH[2]
B7H	reserved	XXH[2]	D7H	reserved	XXH[2]
B8H	**IEN1**[1]	**00H**	**D8H**	**ADCON**[1]	**00H**
B9H	IP1	XX00 0000B[2]	D9H	ADDAT	00H
BAH	reserved	XXH[2])	DAH	DAPR	00H
BBH	reserved	XXH[2])	DBH	P6	XXH[2]
BCH	reserved	XXH[2])	DCH	reserved	XXH[2]
BDH	reserved	XXH[2])	DDH	reserved	XXH[2]
BSH	reserved	XXH[2])	DEH	reserved	XXH[2]
BFH	reserved	XXH[2]	DFH	reserved	XXH[2]
C0H	**IRCON**[1]	**00H**	**E0H**	**ACC**[1]	**00H**
C1H	CCEN	00H	E1H	reserved	XXH[2]
C2H	CCL1	00H	E2H	reserved	XXH[2]
C3H	CCH1	00H	E3H	reserved	XXH[2]
C4H	CCL2	00H	E4H	reserved	XXH[2]
C5H	CCH2	00H	E5H	reserved	XXH[2]
C6H	CCL3	00H	E6H	reserved	XXH[2]
C7H	CCH3	00H	E7H	reserved	XXH[2]
C8H	**T2CON**[1]	**00H**	**E8H**	**P4**[1]	**0FFH**
C9H	reserved	XXH[2]	E9H	reserved	XXH[2]
CAH	CRCL	00H	EAH	reserved	XXH[2]
CBH	CRCH	00H	EBH	reserved	XXH[2]
CCH	TL2	00H	ECH	reserved	XXH[2]
CDH	TH2	00H	EDH	reserved	XXH[2]
CEH	reserved	XXH[2]	EEH	reserved	XXH[2]
CFH	reserved	XXH[2]	EFH	reserved	XXH[2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1:Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B** [1]	**00H**	**F8H**	**P5** [1]	**0FFH**
F1H	reserved	XXH [2]	F9H	reserved	XXH [2]
F2H	reserved	XXH [2]	FAH	reserved	XXH [2]
F3H	reserved	XXH [2]	FBH	reserved	XXH [2]
F4H	reserved	XXH [2]	FCH	reserved	XXH [2]
F5H	reserved	XXH [2]	FDH	reserved	XXH [2]
F6H	reserved	XXH [2]	FEH	reserved	XXH [2]
F7H	reserved	XXH [2]	FFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H** [1]	00H
	B	B-Register	**0F0H** [1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**0D0H** [1]	00H
	SP	Stack Pointer	81H	07H
A/D-Converter	ADCON	A/D Converter Control Register	**0D8H** [1]	00H
	ADDAT	A/D Converter Data Register	0D9H	00H
	DAPR	D/A Converter Program Register	0DAH	00H
Interrupt System	EN0	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0	Interrupt Priority Register 0	0A9H	00H
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000B [3]
	IRCON	Interrupt Request Control Register	**0C0H** [1]	00H
	TCON [2]	Timer Control Register	**88H** [1]	00H
	T2CON [2]	Timer 2 Control Register	**0C8H** [1]	00H
Compare/ Capture- Unit (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCH4	Comp./Capture Reg. 4, High Byte	0CFH	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CCL4	Comp./Capture Reg. 4, Low Byte	0CEH	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON	Timer 2 Control Register	**0C8H** [1]	00H

[1] Bit-addressable special function registers

[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

[3] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Registers- Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80H** [1]	0FFH
	P1	Port 1	**90H** [1]	0FFH
	P2	Port 2	**0A0H** [1]	0FFH
	P3	Port 3	**0B0H** [1]	0FFH
	P4	Port 4	**0E8H** [1]	0FFH
	P5	Port 5	**0F8H** [1]	0FFH
	P6	Port 6, Analog/Digital Input	0DBH	
Pow.Sav.Modes	PCON	Power Control Register	87H	00H
Serial Channels	ADCON [2]	A/D Converter Control Reg.	**0D8H** [1]	00H
	PCON [2]	Power Control Register	87H	00H
	SBUF	Serial Channel Buffer Reg.	99H	0XXH[3]
	SCON	Serial Channel Control Reg.	**98H** [1]	00H
Timer 0/ Timer 1	TCON	Timer Control Register	**88H** [1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1 [2]	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0 [2]	Interrupt Priority Register 0	0A9H	00H
	IP1 [2]	Interrupt Priority Register 1	0B9H	XX00 0000B [3]

[1] Bit-addressable special function registers

[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

[3] X means that the value is indeterminate and the location is reserved

I/O Ports

The SAB 80C515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	$\overline{\text{INT6}}$/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external count or gate input
P3.0	R×D	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	T×D	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The SAB 80C515 has dual-purpose input port. As the ANx lines in the SAB 80515 (NMOS version), the eight port lines at port 6 can be used as analog inputs. But if the input voltages at port 6 meet the specified digital input levels (V_{IL} and V_{IH}), the port can also be used as digital input port. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6.
It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their respective V_{IL}/V_{IH} specifications. Furthermore, it is not possible to use port P6 as output lines. Special function register P6 is located at address 0DBH.

Timer/Counters

The SAB 80C515 contains three 16-bit timers/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 3 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers TL2 and TH2 into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change

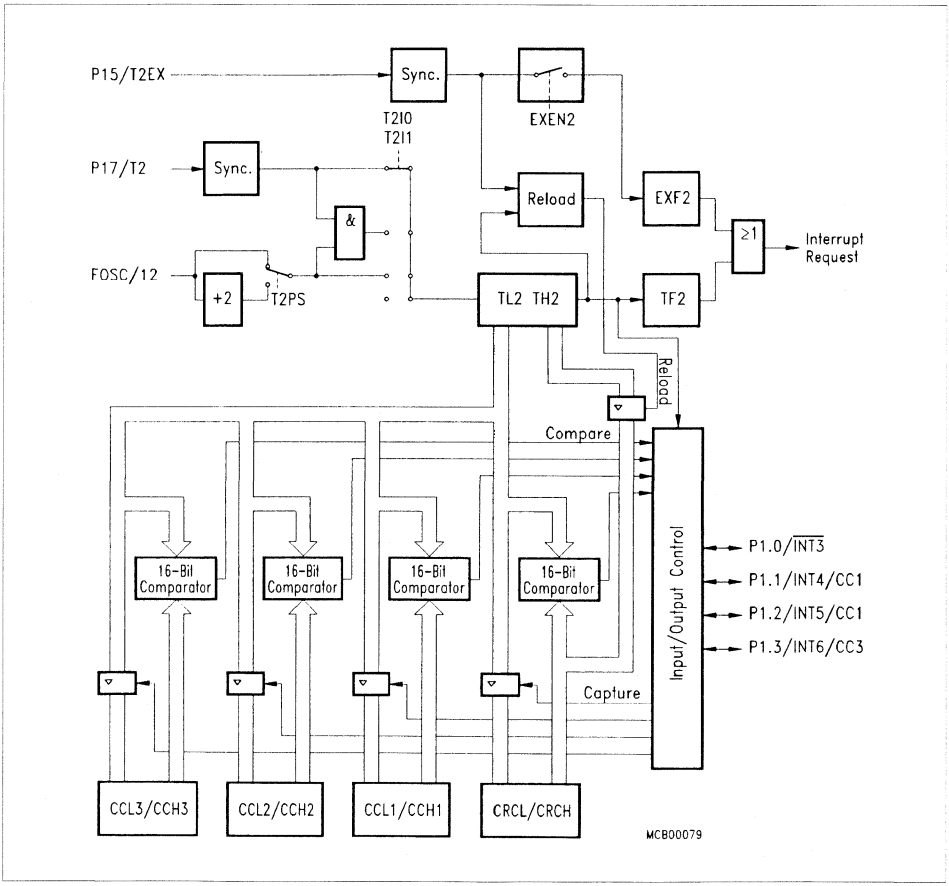


Figure 3
Block Diagram of Timer/Counter 2

Serial Port

The serial port of the SAB 80C515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices.
The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10-bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11-bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11-bits are transmitted (through T×D) or received (through R×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80C515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
There are three characteristic time frames in a conversion cycle (see A/D converter characteristics): the conversion time t_C, which is the time required for one conversion; the sample time t_S which is included in the conversion time and is measured from the start of the conversion; the load time t_L, which in turn is part of the sample time and also is measured from the conversion start.
Within the load time t_L, the analog input capacitance C_I must be loaded to the analog inpult voltage level. For the rest of the sample time t_S, after the load time has passed, the selected analog input must be held constant. During the rest of the conversion time t_C the conversion itself is actually performed. Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution.
In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

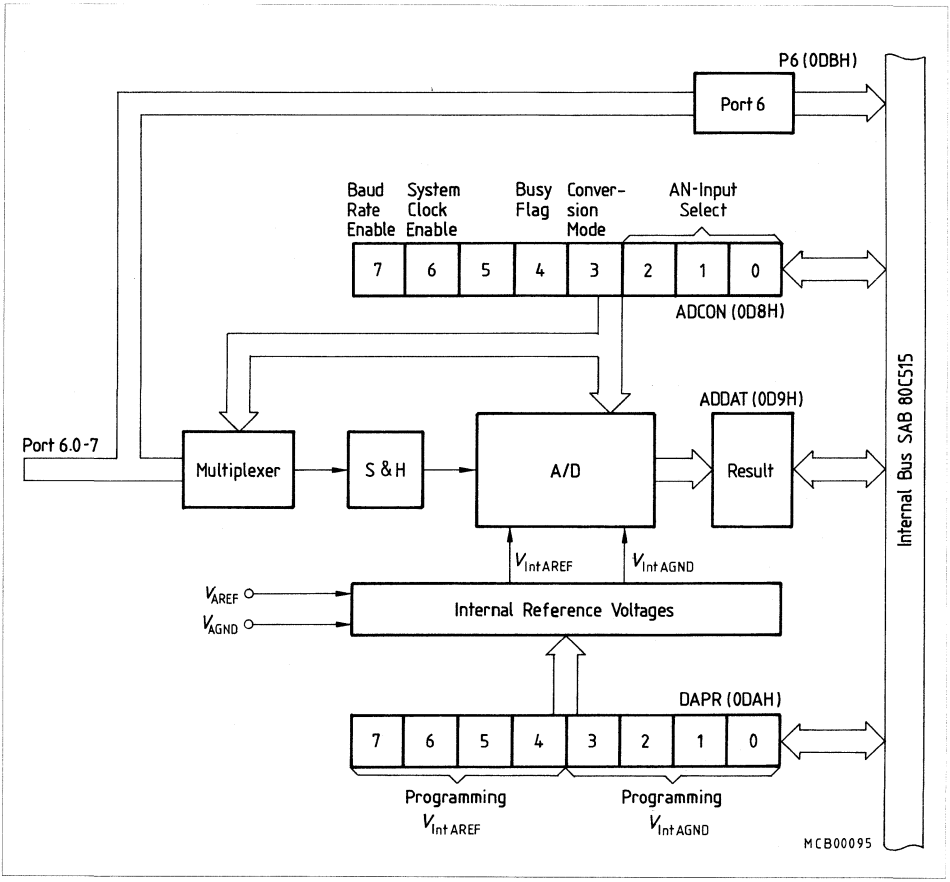


Figure 4
Block Diagram of the A/D Converter

Interrupt Structure

The SAB 80C515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 3
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 interrupt
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 interrupt
RI + TI	0023H	Serial port interrupt
TF2 + EXF2	002BH	Timer 2 interrupt
IADC	0043H	A/D converter interrupt
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

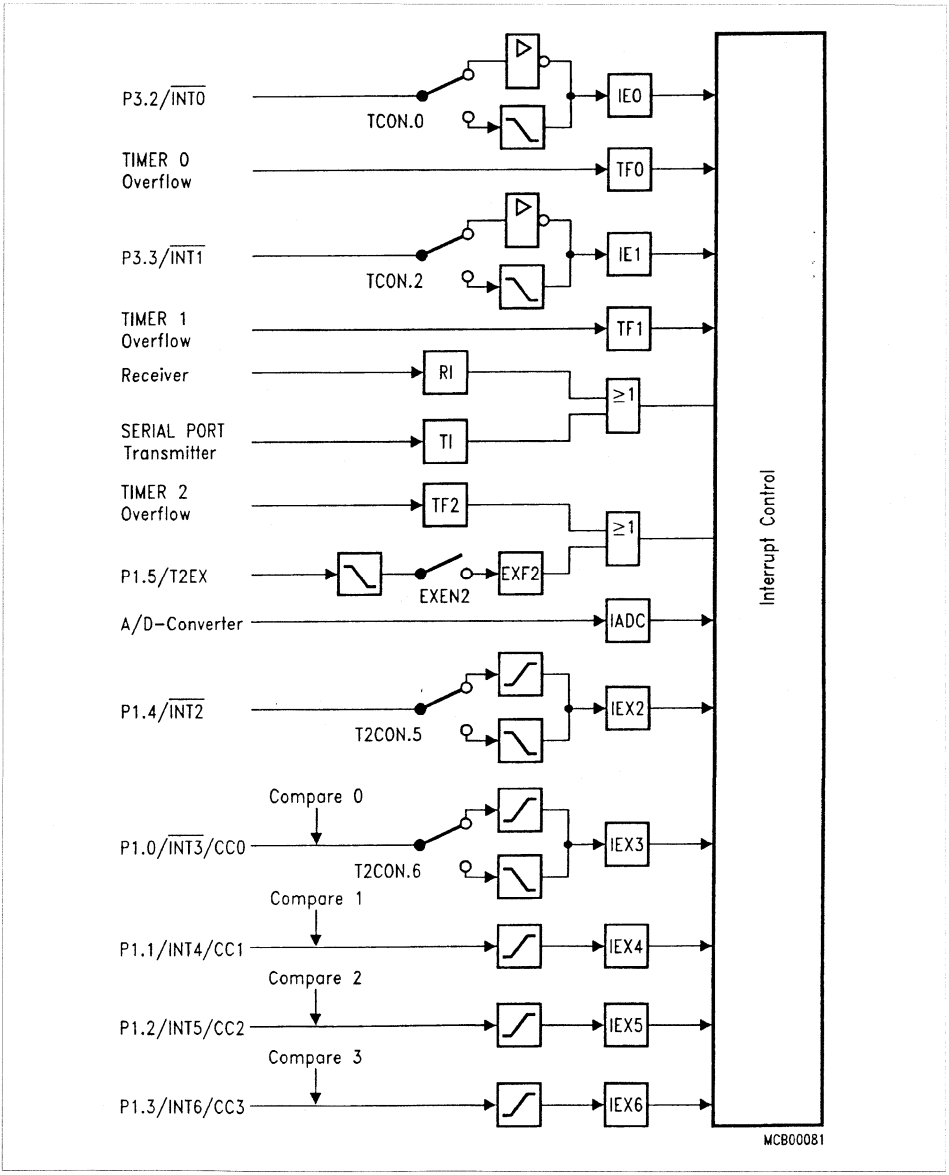


Figure 5
Interrupt Request Sources

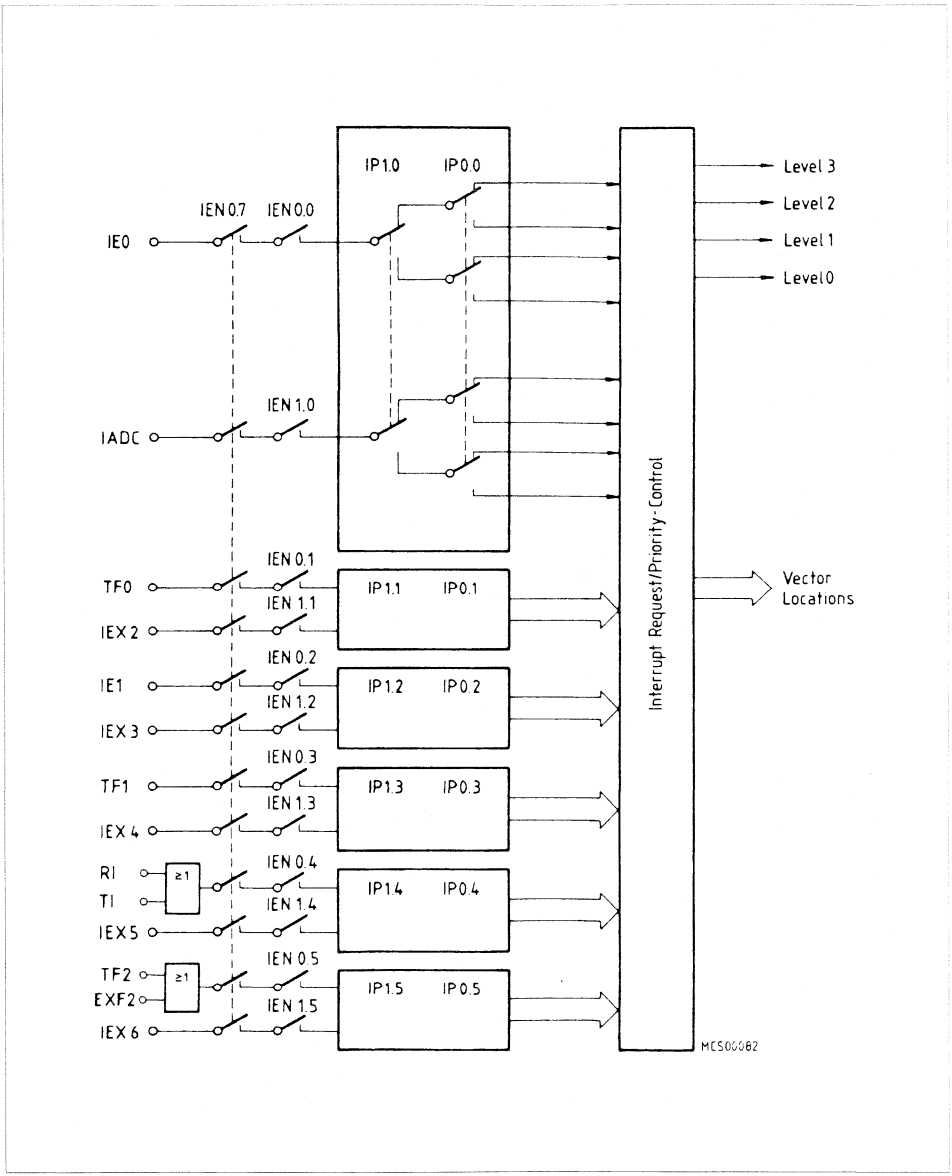


Figure 6
Interrupt Priority Level Structure

Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped during active mode of the device. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes" below).
Therefore, it is possible to use the idle mode in combination with the watchdog timer function. But even the watchdog timer cannot reset the device when one of the power saving modes has been is entered accidentally.
For these reasons several precautions are taken against unintentional entering of the power-down or idle mode (see below).

Power Saving Modes

The ACMOS technology of the SAB 80C515 allows two new power saving modes of the device: The idle mode and the power-down mode. These modes replace the power-down supply mode via pin V_{PD} of the SAB 80515 (NMOS). The SAB 80C515 is supplied via pins V_{CC} also during idle and power-down operation.
However, there are applications where unintentional entering of these power saving modes must be absolutely avoided. Such critical applications often use the watchdog timer to prevent the system from program upsets. Then accidental entering of the power saving modes would even stop the watchdog timer and would circumvent the watchdog timer's task of system protection.

Thus, the SAB 80C515 has an extra pin that allows it to disable both of the power saving modes. When pin $\overline{PE}$ is held high, idle mode and power-down mode are completely disabled and the instruction sequences that are used for entering these modes (see below) will NOT affect the normal operations of the device. When $\overline{PE}$ is held low, the use of the idle mode and power-down mode is possible as described in the following sections.

Pin $\overline{PE}$ has a weak internal pullup resistor. Thus, when left open, the power saving modes are disabled.

The Special Function Register PCON

In the NMOS version SAB 80515 the SFR PCON (address 87H) contains only bit SMOD; in the CMOS version SAB 80C515 there are more bits used (see table 4).
The bits PDE, PDS and IDLE, IDLS select the power-down mode or the idle mode, respectively, when the use of the power saving modes is enabled by pin $\overline{PE}$ (see next page).

If the power-down mode and the idle mode are set at the same time, power-down takes precedence.
Furthermore, register PCON contains two general purpose flags. For example, the flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an idle. Then an instruction that activates Idle can also set one or both flag bits. When idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.
The reset value of PCON is 000X0000B.

Table 4
SFR PCON (87H)

SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	87H
7	6	5	4	3	2	1	0	

Symbol	Position	Function
SMOD	PCON.7	When set, the baud rate of the serial channel in mode 1, 2, 3 is doubled.
PDS	PCON.6	Power-down start bit. The instruction that sets the PDS flag bit is the last instruction before entering the power-down mode.
IDLS	PCON.5	Idle start bit. The instruction that sets the IDLS flag bit is the last instruction before entering the idle mode.
–	PCON.4	Reserved
GF1	PCON.3	General purpose flag
GF0	PCON.2	General purpose flag
PDE	PCON.1	Power-down enable bit. When set, starting of the power-down mode is enabled.
IDLE	PCON.0	Idle mode enable bit. When set, starting of the idle mode is enabled.

Idle Mode

In the idle mode the oscillator of the SAB 80C515 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.

The reduction of power consumption, which can be achieved by this feature depends on the number of peripherals running.

If all timers are stopped and the A/D converter and the serial interface are not running, the maximum power reduction can be achieved. This state is also the test condition for the idle mode I_{CC} (see DC characteristics, note 5).

So the user has to take care which peripheral should continue to run and which has to be stopped during idle mode. Also the state of all port pins – either the pins controlled by their latches or controlled by their secondary functions – depends on the status of the controller when entering idle mode.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. This applies to the compare outputs as well as to the clock output signal or to the serial interface in case it cannot finish reception or transmission during normal operation. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levels (see table 5).

Table 5
Status of External Pins During Idle and Power-Down Mode

	Last instruction executed from internal code memory		Last instruction executed from external code memory	
Outputs	**Idle**	**Power-down**	**Idle**	**Power-down**
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
PORT 0	Data	Data	Float	Float
PORT 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 2	Data	Data	Address	Data
PORT 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 4	Data	Data	Data	Data
PORT 5	Data	Data	Data	Data

As in normal operation mode, the ports can be used as inputs during idle mode. Thus a capture or reload operation can be triggered, the timers can be used to count external events, and external interrupts will be detected.

The idle mode is a useful feature which makes it possible to "freeze" the processor's status – either for a predefined time, or until an external event reverts the controller to normal operation, as discussed below. The watchdog timer is the only peripheral which is automatically stopped during idle mode. If it were not disabled on entering idle mode, the watchdog timer would reset the controller, thus abandoning the idle mode.

When idle mode is used, pin $\overline{PE}$ must be held on low level. The idle mode is then entered by two consecutive instructions. The first instruction sets the flag bit IDLE (PCON.0) and must not set bit IDLS (PCON.5), the following instruction sets the start bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). The hardware ensures that a concurrent setting of both bits, IDLE and IDLS, does not initiate the idle mode. Bits IDLE and IDLS will automatically be cleared after being set. If one of these register bits is read the value that appears is 0 (see table 4). This double instruction is implemented to minimize the chance of an unintentional entering of the idle mode which would leave the watchdog timer's task of system protection without effect.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the idle mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000001B     ;Set bit IDLE, bit IDLS must not be set
ORL     PCON,#00100000B     ;Set bit IDLS, bit IDLE must not be set
```

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enable interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.

- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Power-Down Mode

In the power-down mode, the on-chip oscillator is stopped. Therefore all functions are stopped; only the contents of the on-chip RAM and the SFR's are maintained.The port pins controlled by their port latches output the values that are held by their SFR's.
The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power-down mode; when the clockout signal (CLKOUT, P1.6) is enabled, it will stop at low level. ALE and $\overline{PSEN}$ hold at logic low level (see table 5).

To enter the power-down mode the pin $\overline{PE}$ must be on low level. The power-down mode then is entered by two consecutive instructions. The first instruction has to set the flag bit PDE (PCON.1) and must not set bit PDS (PCON.6), the following instruction has to set the start bit PDS (PCON.6) and must not set bit PDE (PCON.1). The hardware ensures that a concurrent setting of both bits, PDE and PDS, does not initiate the power-down mode. Bits PDE and PDS will automatically be cleared after having been set and the value shown by reading one of these bits is always 0 (see table 4). This double instruction is implemented to minimize the chance of unintentionally entering the power-down mode which could possibly "freeze" the chip's activity in an undesired status.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the power-down mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000010B   ;Set bit PDE, bit PDS must not be set
ORL     PCON,#01000000B   ;Set bit PDS, bit PDE must not be set
```

The instruction that sets bit PDS is the last instruction executed before going into power-down mode.

The only exit from power-down mode is a hardware reset. Reset will redefine all SFR's, but will not change the contents of the internal RAM.

In the power-down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power- down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power-down mode is terminated. The reset signal that terminates the power-down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Differences in Pin Assignments of the SAB 80C515 and SAB 80515

Since the SAB 80C515 is designed in CMOS technology, this device requires no V_{BB} pin, because the die's substrate is internally connected to V_{CC}.

Furthermore, the RAM backup power supply via pin V_{PD} is replaced by the software- controlled power-down mode and power supply via V_{CC}.

Therefore, pins V_{BB} and V_{PD} of the NMOS version SAB 80515 are used for other functions in the SAB 80C515.

Pin 4 (the former pin V_{PD}) is the new $\overline{PE}$ pin which enables the use of the power saving modes.

Pin 37 (the former pin V_{BB}) becomes an additional V_{CC} pin. Thus, it is possible to insert a decoupling capacitor between pin 37 (V_{CC}) and pin 38 (V_{SS}) very close to the device, thereby avoiding long wiring and reducing the voltage distortion resulting from high dynamic current peaks.

There is a difference between the NMOS and CMOS version concerning the clock circuitry. When the device is driven from an external source, pin XTAL2 must be driven by the clock signal; pin XTAL1, however, must be left open in the SAB 80C515 (must be tied low in the NMOS version). When using the oscillator with a crystal there is no difference in the circuitry.

Thus, due to its pin compatibility the SAB 80C515 normally substitutes any SAB 80515 without redesign of the user's printed circuit board, but the user has to take care that the two V_{CC} pins are hardwired on-chip. In any case, it is recommended that power is supplied on both V_{CC} pins of the SAB 80C515 to improve the power supply to the chip.
If the power saving modes are to be used, pin $\overline{PE}$ must be tied low, otherwise these modes are disabled.

Instruction Set

The SAB 80C515 / 83C535 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6579-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80C515 ..... 0 to 70 °C
SAB 80C515-T3 ..... – 40 to 85 °C
SAB 80C515-T4 ..... – 40 to 110 °C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... –10mA to +10mA
Absolute sum of all input currents during overload condition ..... I100mA I
Power disipation 2W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values defined by the absolute maximum ratings.*

DC Characteristics

$V_{CC} = 5\ V \pm 10\ \%$; $V_{SS} = 0\ V$

T_A = to 70 °C for the SAB 80C515/80C535
T_A = – 40 to 85 °C for the SAB 80C515/80C535-T3
T_A = – 40 to 110 °C for the SAB 80C515/80535-T4

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input high voltage (except $\overline{RESET}$ and XTAL2)	V_{IH}	2.0 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	– 0.45	V	I_{OL} = 1.6 mA [1]

Notes see page 148

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA 1)
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 mA I_{OH} = – 10 mA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 400 mA I_{OH} = – 40 mA 2)
Logic 0 input current, ports 1, 2, 3, 4, 5	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
Input low current ($\overline{XTAL2}$)	I_{IL3}	–	–15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, EA)	I_{LI}	–	± 10	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25°C
Power-supply current: Active mode, 12 MHz 6) Idle mode, 12 MHz 6) Active mode, 16 MHz 6) Idle mode, 16 MHz 6) Power-down mode	 $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{PD}$	 – – – – –	 35 13 46 17 50	 mA mA mA mA µA	 V_{CC} = 5 V 4) V_{CC} = 5 V 5) V_{CC} = 5 V 4) V_{CC} = 5 V 5) V_{CC} = 2 V to 5.5 V 3)

Notes see page 148

Notes (for page 146 and 147)

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V.
Then, it may be desirable to qualify ALE with a Schmitttrigger, or use an address latch with a Schmitttrigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the VOH on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

3) Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = Port 6 = V_{CC};
XTAL1 = N.C.; XTAL2 = V_{SS}; $\overline{RESET}$ = V_{CC}; V_{AGND} = V_{SS}; all other pins are disconnected.

4) I_{CC}(active mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; EA = Port 0 = Port 6 = V_{CC}; RESET = V_{SS}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = Port 6 V_{CC}; RESET = V_{CC}; all other pins are disconnected; all on-chip peripherals are disabled.

6) I_{CC} at other frequencies is given by:
Active mode: $I_{CC\,max}$ (mA) = 2.67 × f_{OSC} (MHz) + 3.00
Idle mode: $I_{CC\,max}$ (mA) = 0.88 × f_{OSC} (MHz) + 2.50
where f_{OSC} is the oscillator frequency in MHz.
$I_{CC\,max}$ is given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5)

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS}= 0 V; V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to 70°C for SAB 80C515/80C535
T_A= – 40 to 85°C for SAB 80C515/80C535-T40/85
T_A= – 40 to 110°C for SAB 80C515/80C535-T40/110

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
Analog input capacitance	C_I	–	25	45	pF	7)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	7t_{CY}	µs	–
Conversion time (incl. sample time)	t_C	–	–	13 t_{CY}	µs	–
Differential non-linearity	DNLE	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
Integral non-linearity	INLE	–	± 1/2	± 1	LSB	V_{AREF} = V_{CC}
Offset error			± 1/2	± 1	LSB	$V_{IntAGND}$ =
Gain error		–	± 1/2	± 1	LSB	V_{AGND} = V_{SS}7)
Total unadjusted error	TUE		± 1	± 2	LSB	
V_{AREF} supply current	I_{REF}	–	–	5	mA	8)
Internal reference error	$V_{Int\ REFERR}$	–		± 30	mV	8)

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S)

8) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding these limit values at one or more input channels will cause additional current which is sinked / sourced at these channels. This may also affect the accuracy of other channels which are operated within these specifications.

AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF;
C_L for all outputs = 80 pF); T_A = 0 to 70°C for SAB 80C515/80C535
T_A = – 40 to 85°C for SAB 80C515/80C535-T40/85
T_A = – 40 to 110°C for SAB 80C515/80C535-T40/110

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	53	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	48	–	$t_{CLCL} - 35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215		$3t_{CLCL} - 35$		ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} [1]	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} [1]	75		$t_{CLCL} - 8$		ns
Address to valid instruction in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

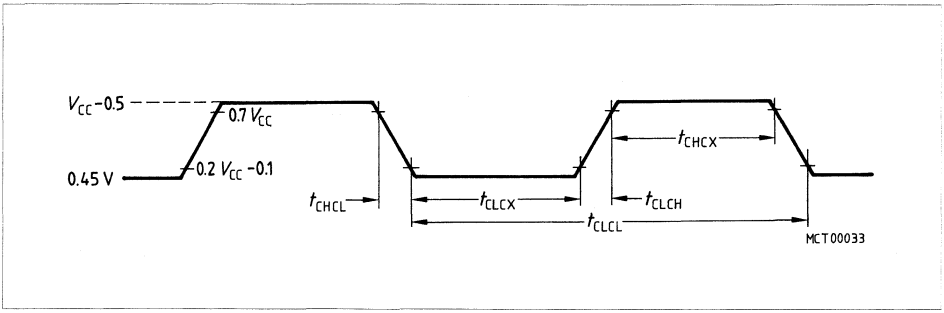
[1] Interfacing the SAB 80C515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6\,t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6\,t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2\,t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5\,t_{CLCL} - 165$	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2\,t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8\,t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9\,t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3\,t_{CLCL} - 50$	$3\,t_{CLCL} + 50$	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	$4\,t_{CLCL} - 130$	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	$7\,t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

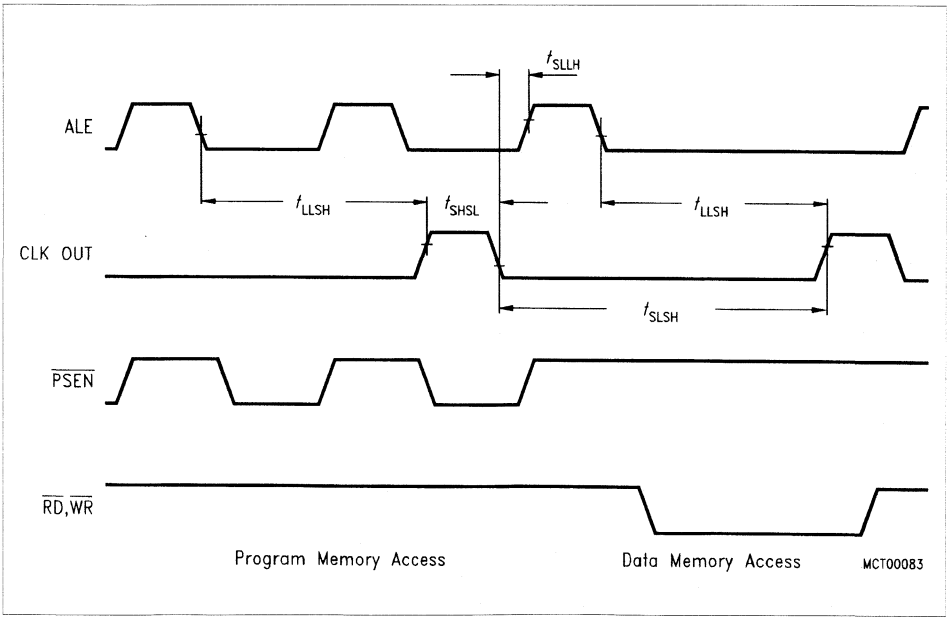
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 12 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	83.3	2000	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



System Clock Timing

AC Characteristics for SAB 80C515-16/80C535-16

V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF;
C_L for all outputs = 80 pF) T_A = 0 to 70°C for SAB 80C515-16/80C535-16
T_A = – 40 to 85°C for SAB 80C515-16/80C535-16-T40/85

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 16 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	$2\,t_{CLCL}-40$	–	ns
Address setup to ALE	t_{AVLL}	33	–	$t_{CLCL}-30$	–	ns
Address hold after ALE	t_{LLAX}	28	–	$t_{CLCL}-35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	150	–	$4\,t_{CLCL}-100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	–	$t_{CLCL}-25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153		$3\,t_{CLCL}-35$		ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	88	–	$3t_{CLCL}-100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} [1]	–	43	–	$t_{CLCL}-20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} [1]	55		$t_{CLCL}-8$		ns
Address to valid instruction in	t_{AVIV}	–	198	–	$5t_{CLCL}-115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

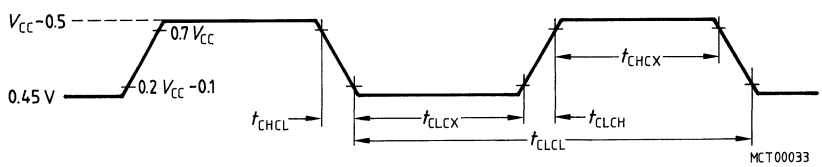
[1] Interfacing the SAB 80C515-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 16 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

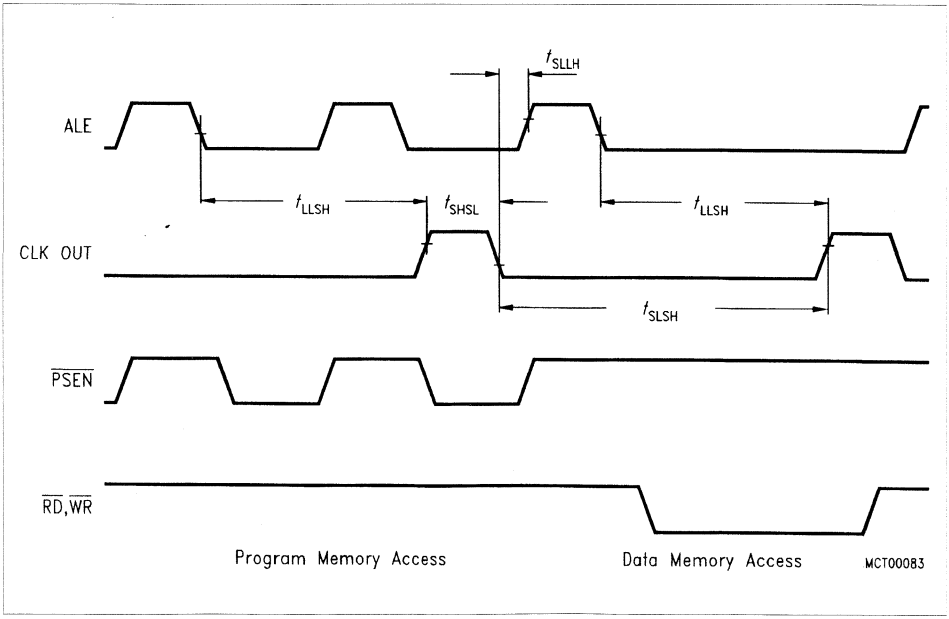
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 16 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	62.5	2000	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	16	MHz
High time	t_{CHCX}	15	–	ns
Low time	t_{CLCX}	15	–	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 16 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLK OUT	t_{LLSH}	398	–	$7t_{CLCL} - 40$	–	ns
CLK OUT high time	t_{SHSL}	85	–	$2t_{CLCL} - 40$	–	ns
CLK OUT low time	t_{SLSH}	585	–	$10\,t_{CLCL} - 40$	–	ns
CLK OUT low to ALE high	t_{SLLH}	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

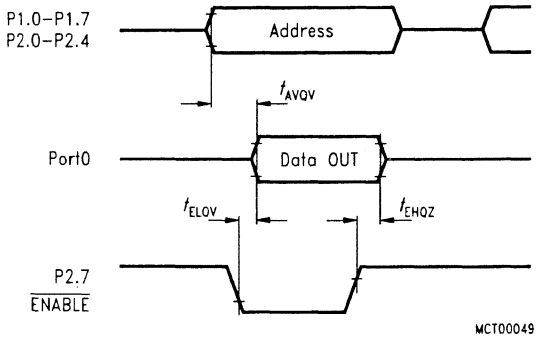


System Clock Timing

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	
ROM Verification				
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL1}$	4	6	MHz
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns

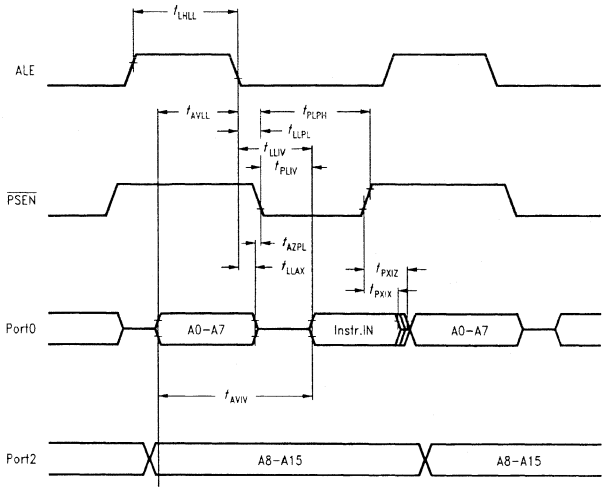


Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

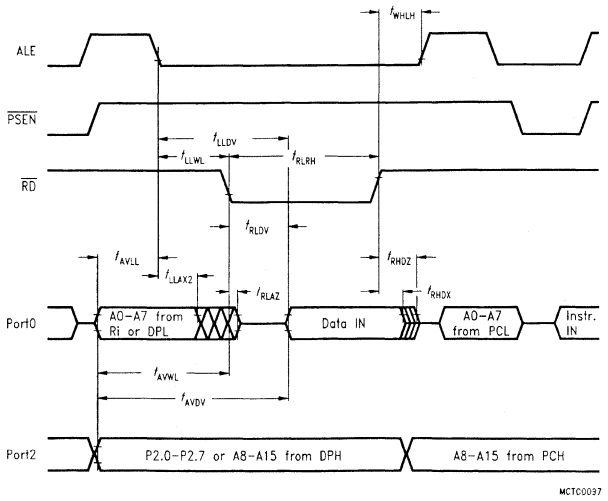
Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

ROM Verification

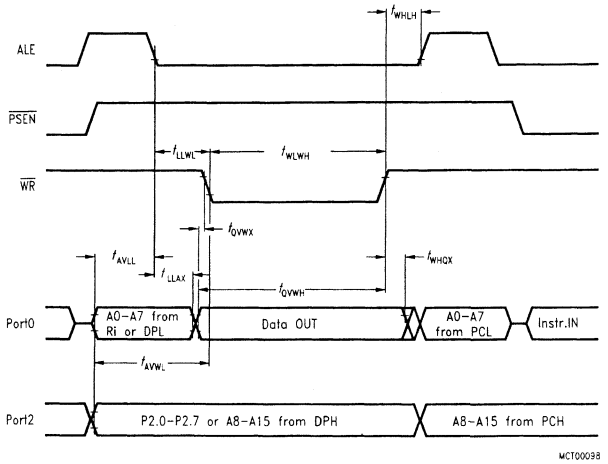
Waveforms



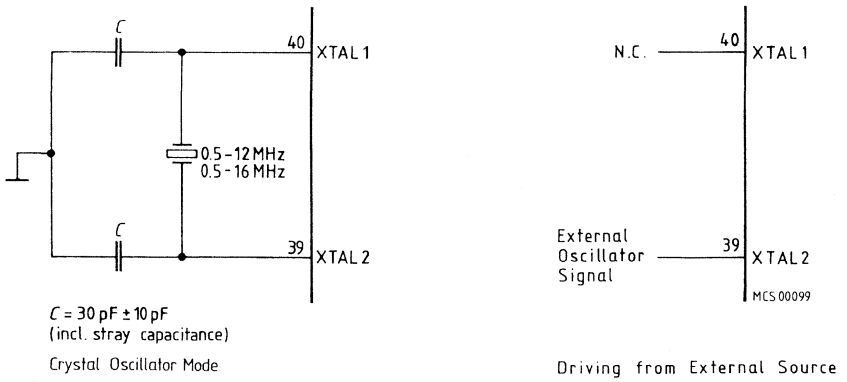
Program Memory Read Cycle



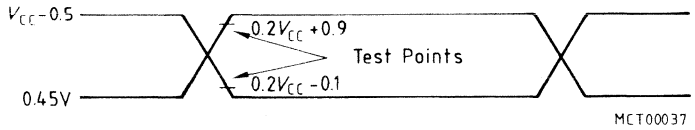
Data Memory Read Cycle



Data Memory Write Cycle

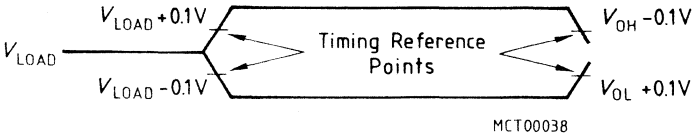


Recommended Oscillator Circuits



AC inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at $V_{IH\ min}$ for a logic '1' and $V_{IL\ max}$ for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV deviation from the load voltage V_{OH}/V_{OL} occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

SAB 80C515A / 83C515A-5

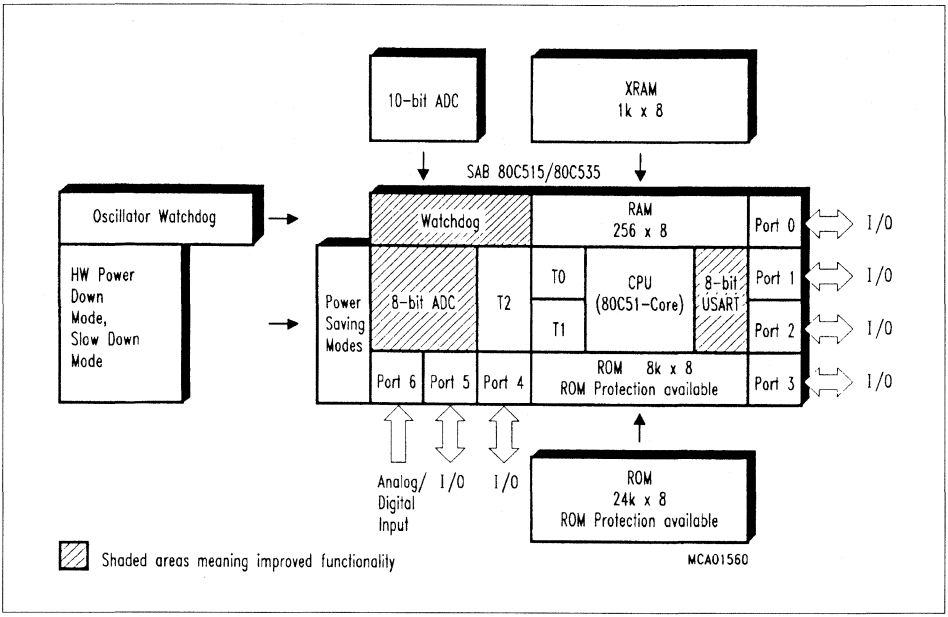
Preliminary

SAB 83C515A-5	Microcontroller with factory mask-programmable ROM
SAB 80C515A	Microcontroller for external ROM

- SAB 80C515A / 83C515A-5, up to 18 MHz operation frequency
- 32 K × 8 ROM (SAB 83C515A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- Additional 1 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  1 µs instruction cycle time at 12 MHz
  666 ns instruction cycle time at 18 MHz
  256 directly addressable bits
  Boolean processor
  64 Kbyte external data and program memory addressing
- Three 16-bit timer/counters
- Versatile "fail-safe" provisions
- Twelve interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 8 multiplexed inputs
- Full duplex serial interface with programmable Baudrate-Generator
- Functionally compatible with SAB 80C515
- Extended power saving mode
- Fast Power-On Reset
- Six ports: 48 I/O lines, 8 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85°C (T3)
  – 40 to 110°C (T4)
- Plastic package: P-LCC-68

The SAB 80C515A/83C515A-5 is a high-end member of the Siemens SAB 8051 microcontroller family. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

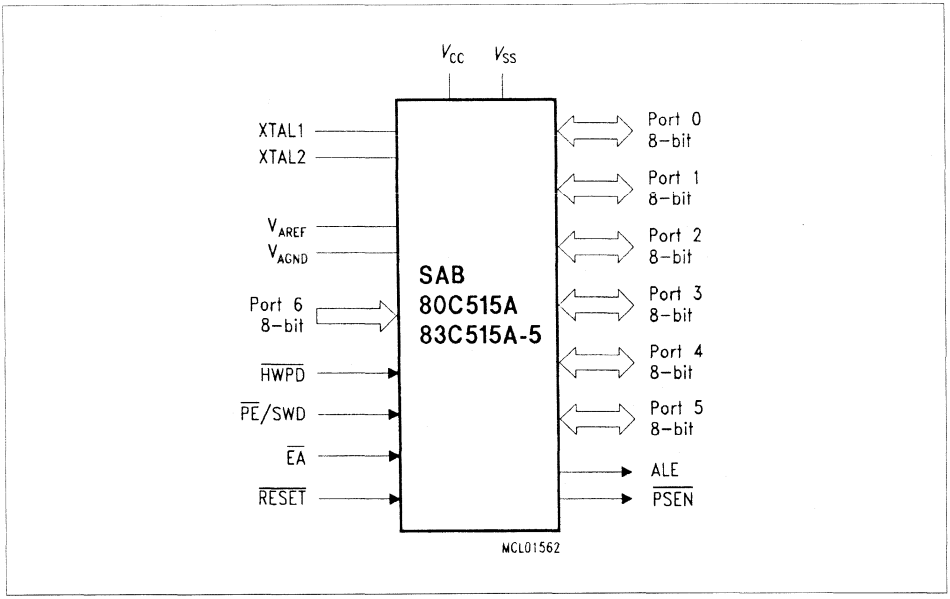
While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C515A/83C515A-5 contains more on-chip RAM/ROM. Furthermore a new 10-bit A/D-Converter is implemented as well as extended security mechanisms. The SAB 80C515A is identical with the SAB 83C515A-5 except that it lacks the on-chip program memory. The SAB 80C515A / 83C515A-5 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC- 68).



Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C515A-N18	Q67120-C581	P-LCC-68	for external memory,18 MHz
SAB 83C515A-5N18	Q67120-C580	P-LCC-68	with mask-programmable ROM, 18 MHz
SAB 80C515A-N18-T3	Q67120-C784	P-LCC-68	for external memory,18 MHz ext. temperature – 40 to 85 °C
SAB 83C515A-5N18-T3	Q67120-C787	P-LCC-68	with mask-programmable ROM, 18 MHz ext. temperature – 40 to 85 °C

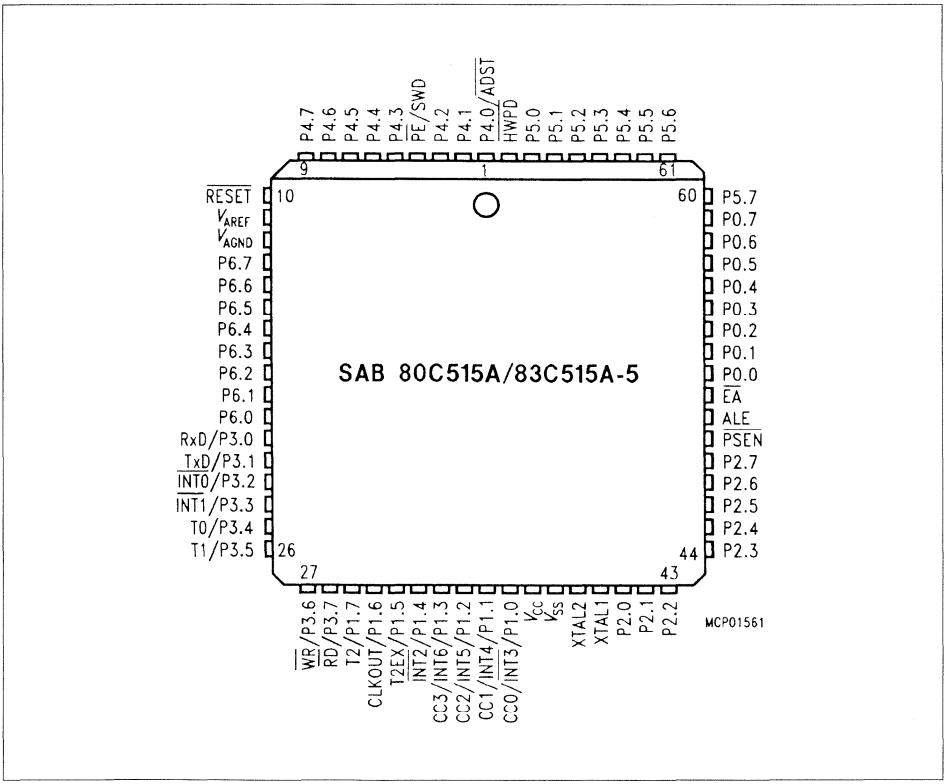
Extended temperature range T4 (– 40 to 110 °C) on request .



Logic Symbol

The pin functions of the SAB 80C515A are identical with those of the SAB 80C515 with following exception:

Pin	SAB 80C515A	SAB 80C515
68	$\overline{\text{HPWD}}$	V_{CC}
1	P0.4/$\overline{\text{ADST}}$	P4.0
4	$\overline{\text{PE}}$/SWD	$\overline{\text{PE}}$



Pin Configuration
(P-LCC-68)

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary function assigned to port 6: – $\overline{ADST}$(P4.0): external A/D converter start pin
$\overline{PE}$/SWD	4	I	**Power saving mode $\overline{enable}$/Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
$\overline{RESET}$	10	I	**$\overline{Reset}$ pin** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515A. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF1}	11		**Reference voltage** for the A/D converter
V_{AGND}	12		**Reference ground** for the A/D converter

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P6.7-P6.0	13-20	I	**Port 6** is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications high/low input voltages, and for the eight multiplexed analog inputs.
P3.0-P3.7	21-28	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$(P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{INT2}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
XTAL2	39	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
XTAL1	40	-	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be taken into account.
P2.0-P2.7	41- 48	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	O	The **Address Latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{EA}$	51	I	**External Access Enable** When held high, the SAB 80C515A executes instructions from the internal ROM as long as the PC is less than 8192. When held low, the SAB 80C515A fetches all instructions from external program memory. For the SAB 80C535A this pin must be tied low.
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515A. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
$\overline{HWDP}$	68	I	**Hardware Power Down** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C515A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (**see table 5**)
V_{CC}	37		**Supply voltage** during normal, idle, and power-down operation.
V_{SS}	38		**Ground** (0 V)

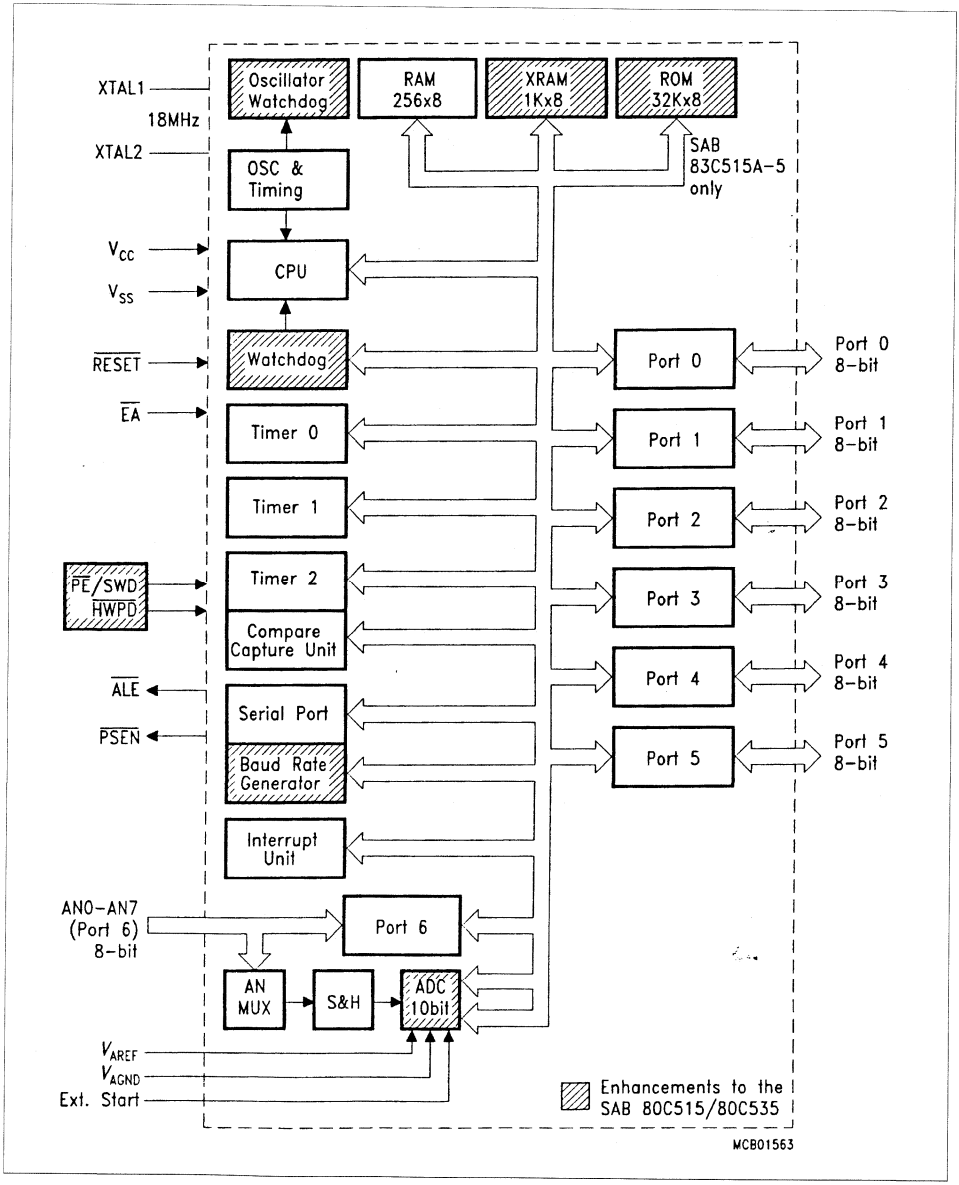


Figure 1
Block Diagram

Functional Description

The SAB 80C515A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C515. The SAB 80C515A is therefore code compatible with the SAB 80C515.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C515A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

While maintaining all architectural and operational characteristics of the SAB 80C515 the SAB 80C515A incorporates more on-chip RAM. A new 10-bit A/D-Converter is implemented as well as an oscillator watchdog unit. Also the maximum operating frequency of 18 MHz is higher than at the SAB 80C515.

With exception of the ROM sizes both parts are identical. Therefore the therm SAB 80C515A refers to both versions within this specification unless otherwise noted.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C515A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

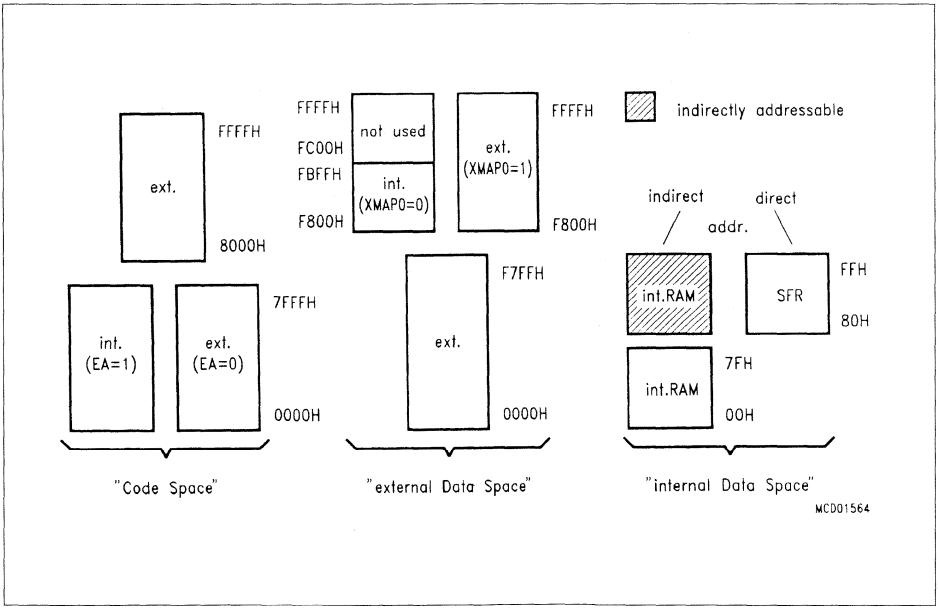


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C515A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C515A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ determines whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C515A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask. Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	ROM-Verification Mode (see 'AC Characteristics')	Restrictions
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Data Space')

The data memory space consists of an internal and an external memory space.The SAB 80C515A contains another 1 Kbyte on On-Chip RAM additional to the 256-bytes internal RAM of the base type SAB 80C515. This RAM is called XRAM ('extended RAM') in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by a 16-bit datapointer. Registers XPAGE and SYSCON are controlling whether data fetches at addresses F800H to FBFFH are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

- the lower 128 bytes of RAM including four register banks containing eight registers each
- the upper 128 byte of RAM
- the 128 byte special function register area.
- a 1 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from F800H to FBFFH. Special Function Register SYSCON controls whether data is read from or written to XRAM or external RAM.

A map of the internal data memory is shown in figure 2. The overlapping address spaces of the standard internal data memory (256 byte) are accessed by different addressing modes (see User's Manual SAB 80C515). The stack can be located anywhere in the internal data memory.

Architecture of the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range (F800H-FBFFH). Nevertheless when XRAM is enabled the address range F800H to FFFFH is occupied. This is done to assure software compatibility to SAB 80C517A. It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C515A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR ≥ F800H).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C515A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91H									XPAGE

The reset value of XPAGE is 00H.
XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C515A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM: The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.

b) Access to external memory: The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C515A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. 0B1H							XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 =0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for / $\overline{RD}$/$\overline{WR}$signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is XXXX XX01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C515A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the external $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

   I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

Table 1:
Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	DPTR ≥ XRAM address range	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/C b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	XPAGE ≥ XRAM addr. page range	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/C b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used

modes compatible to 8051 - family

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 2 and table 3.

In table 2 they are organized in numeric order of their addresses. In table 3 they are organized in groups which refer to the functional blocks of the SAB 80C515A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**S0CON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXH [2]
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	(WDTL)		9CH	reserved	XXH [2]
85H	(WDTH)		9DH	reserved	XXH [2]
86H	WDTREL	00H	9EH	reserved	XXH [2]
87H	PCON	00H	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	XPAGE	XXH [2]	A9H	IP0	00H
92H	reserved	XXH [2]	AAH	SRELL	0D9H
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3** [1]	**0FFH**	**D0H**	**PSW** [1]	**00H**
B1H	SYSCON	XXXX XX01B [2]	D1H	reserved	XXH [2]
B2H	reserved	XXH [2]	D2H	reserved	XXH [2]
B3H	reserved	XXH [2]	D3H	reserved	XXH [2]
B4H	reserved	XXH [2]	D4H	reserved	XXH [2]
B5H	reserved	XXH [2]	D5H	reserved	XXH [2]
B6H	reserved	XXH [2]	D6H	reserved	XXH [2]
B7H	reserved	XXH [2]	D7H	reserved	XXH [2]
B8H	**EN1** [1]	**00H**	**D8H**	**ADCON0** [1]	**00H**
B9H	IP1	XX00 0000B [2]	D9H	ADDATH	00H
BAH	SRELH	XXXX XX11B [2]	DAH	ADDATL	00H
BBH	reserved	XXH [2]	DBH	P6	XXH [2]
BCH	reserved	XXH [2]	DVH	ADCVON1	XXXX 0000B [2]
BDH	reserved	XXH [2]	DDH	reserved	XXH [2]
BEH	reserved	XXH [2]	DEH	reserved	XXH [2]
BFH	reserved	XXH [2]	DFH	reserved	XXH [2]
C0H	**IRCON** [1]	**00H**	**E0H**	**ACC** [1]	**00H**
C1H	CCEN	00H	E1H	reserved	XXH [2]
C2H	CCL1	00H	E2H	reserved	XXH [2]
C3H	CCH1	00H	E3H	reserved	XXH [2]
C4H	CCL2	00H	E4H	reserved	XXH [2]
C5H	CCH2	00H	E5H	reserved	XXH [2]
C6H	CCL3	00H	E6H	reserved	XXH [2]
C7H	CCH3	00H	E7H	reserved	XXH [2]
C8H	**T2CON** [1]	**00H**	**E8H**	**P4** [1]	**0FFH**
C9H	reserved	XXH [2]	E9H	reserved	XXH [2]
CAH	CRCL	00H	EAH	reserved	XXH [2]
CBH	CRCH	00H	EBH	reserved	XXH [2]
CCH	TL2	00H	ECH	reserved	XXH [2]
CDH	TH2	00H	EDH	reserved	XXH [2]
CEH	reserved	XXH [2]	EEH	reserved	XXH [2]
CFH	reserved	XXH [2]	EFH	reserved	XXH [2]

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B** [1]	**00H**	**F8H**	P5 [1]	**00FH**
F1H	reserved	XXH [2]	F9H	reserved	XXH [2]
F2H	reserved	XXH [2]	FAH	reserved	XXH [2]
F3H	reserved	XXH [2]	FBH		
F4H	reserved	XXH [2]	FCH		
F5H	reserved	XXH [2]	FDH		
F6H	reserved	XXH [2]	FEH		
F7H	reserved	XXH [2]	FFH		

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H** [1]	00H
	B	B-Register	**0F0H** [1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**0D0H** [1]	00H
	SP	Stack Pointer	81H	07H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**0D8H** [1]	00H
	ADCON1	A/D Converter Control Register 1	0DCH	0XXX 0000B [3]
	ADDATH	A/D Converter Data Reg. High Byte	0D9H	00H
	ADDATL	A/D Converter Data Reg. Low Byte	0DAH	00H
Interrupt System	EN0	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0	Interrupt Priority Register 0	0A9H	00H
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000B
	IRCON0	Interrupt Request Control Register	**0C0H** [1]	00H
	TCON [2]	Timer Control Register	**88H** [1]	00H
	T2CON [2]	Timer 2 Control Register	**0C8H**	00H
Compare/ Capture- Unit (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCH4	Comp./Capture Reg. 4, High Byte	0CFH	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CCL4	Comp./Capture Reg. 4, Low Byte	0CEH	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON	Timer 2 Control Register	**0C8H** [1]	00H
XRAM	XPAGE	Page Address Register for Extended On Chip RAM	91H	00H
	SYSCON	XRAM Control Register	0B1H	XXXX XX01B [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80H** 1)	0FFH
	P1	Port 1	**90H** 1)	0FFH
	P2	Port 2	**0A0H** 1)	0FFH
	P3	Port 3	**0B0H** 1)	0FFH
	P4	Port 4	**0E8H** 1)	0FFH
	P5	Port 5	**0F8H** 1)	0FFH
	P6	Port 6, Analog/Digital Input	0DBH	
Pow.Sav. Mode	PCON	Power Control Register	87H	00H
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	**0D8H** 1)	00H
	PCON 2)	Power Control Register	87H	00H
	SBUF	Serial Channel Buffer Reg.	99H	0XXH 3)
	SCON	Serial Channel Control Reg.	**98H** 1)	00H
	SRELL	Serial Channel Reload Reg., low byte	AAH	D9H
	SRELH	Serial Channel Reload Reg., high byte	BAH	XXXX XX11B 3)
Timer 0/ Timer 1	TCON	Timer Control Register	**88H** 1)	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**0A8H** 1)	00H
	IEN1 2)	Interrupt Enable Register 1	**0B8H** 1)	00H
	IP0 2)	Interrupt Priority Register 0	0A9H	00H
	IP1 2)	Interrupt Priority Register 1	0B9H	XX00 0000B
	WDTREL	Watchdog Timer Reload Reg.	86H	00H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C515A a new high performance / high-speed 8-channel 10-bit A/D-Converter (ADC) is implemented. Its successive approximation technique provides 7 µs conversion time (f_{OSC} = 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C515. The main functional blocks are shown in figure 3.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler.

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.3
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	1.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

The ADC is clocked (f_{ADC}) with f_{OSC}/8. Because of the ADC's maximum clock frequency of 2 MHz the prescaler (divide-by-2) has to be enabled (set Bit ADCL in SFR ADCON 1) when the oscillator frequency (f_{OSC}) is higher than 16 MHz.

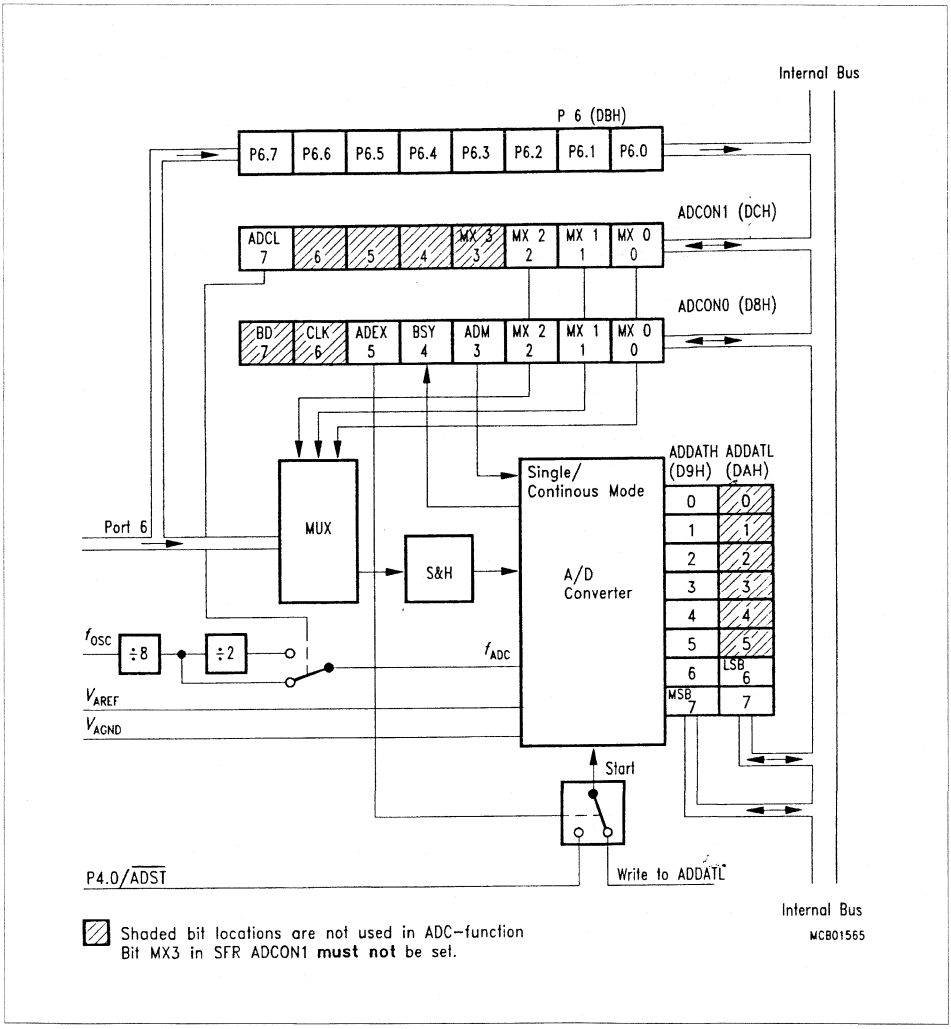


Figure 3
Block Diagram A/D Converter

Timers /Counters

The SAB 80C515A contains three 16-bit timers/counters wich are useful in many applications for timing and counting. the input clock for wach timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515A is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 4 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers TL2 and TH2 into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

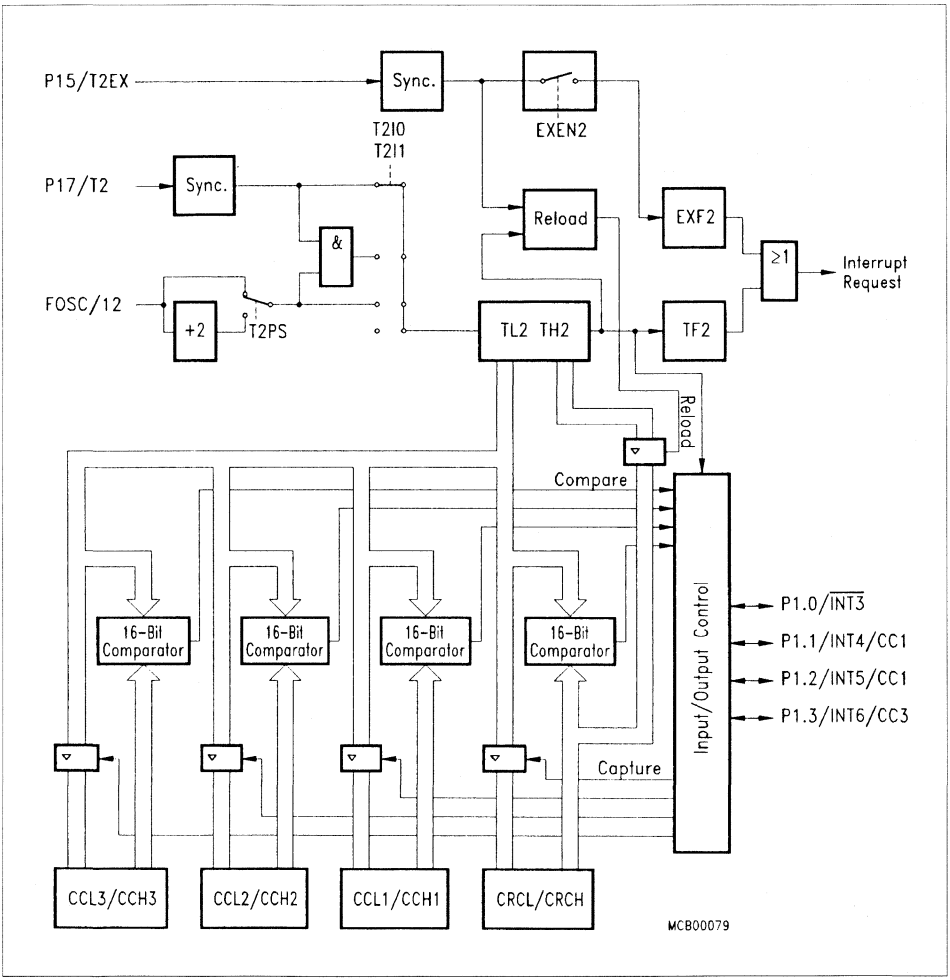


Figure 4
Block Diagram of Timer/Counter 2

Interrupt Structure

The SAB 80C515A has 12 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 interrupt
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 interrupt
RI + TI	0023H	Serial port interrupt
TF2 + EXF2	002BH	Timer 2 interrupt
IADC	0043H	A/D converter interrupt
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles, if no other interrrupt of the same or a higher priority level is in process.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

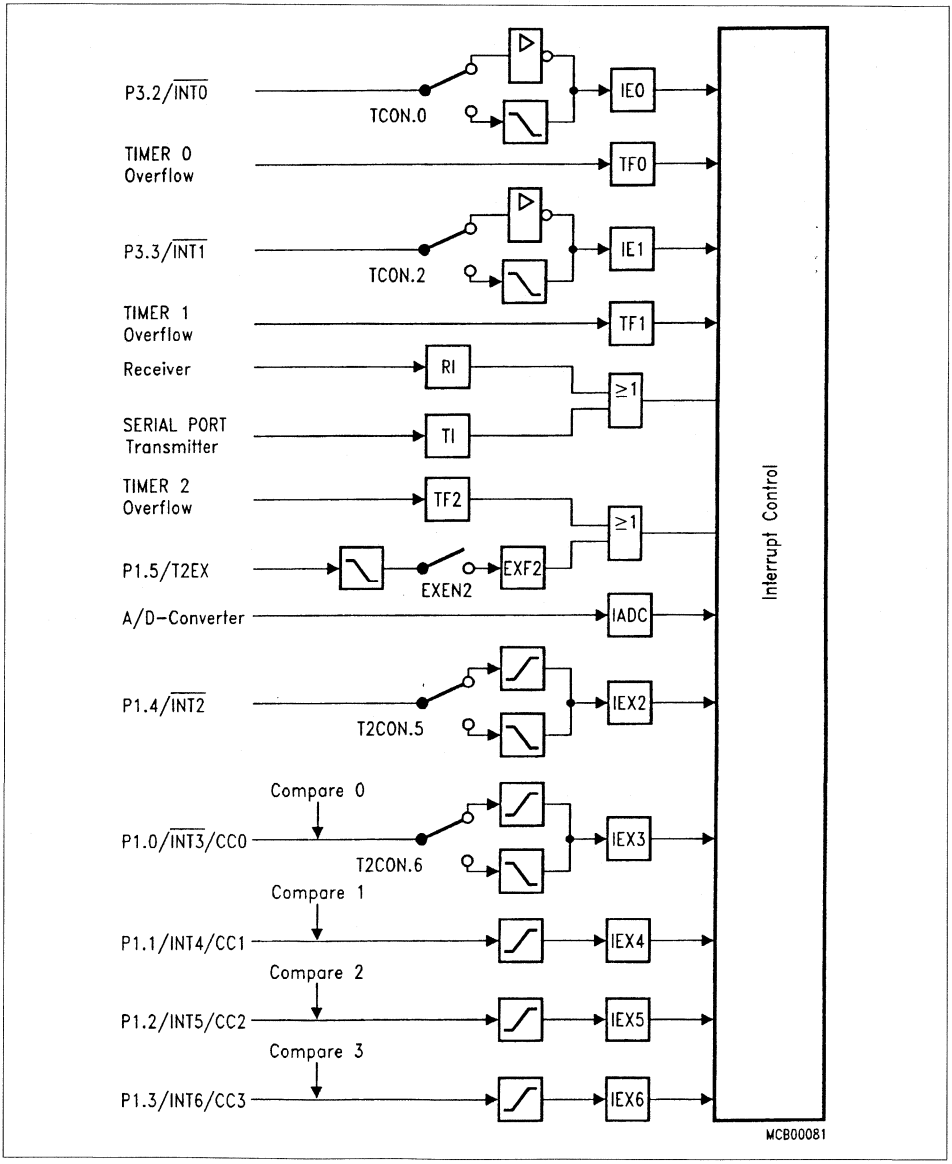


Figure 5
Interrupt Request Sources

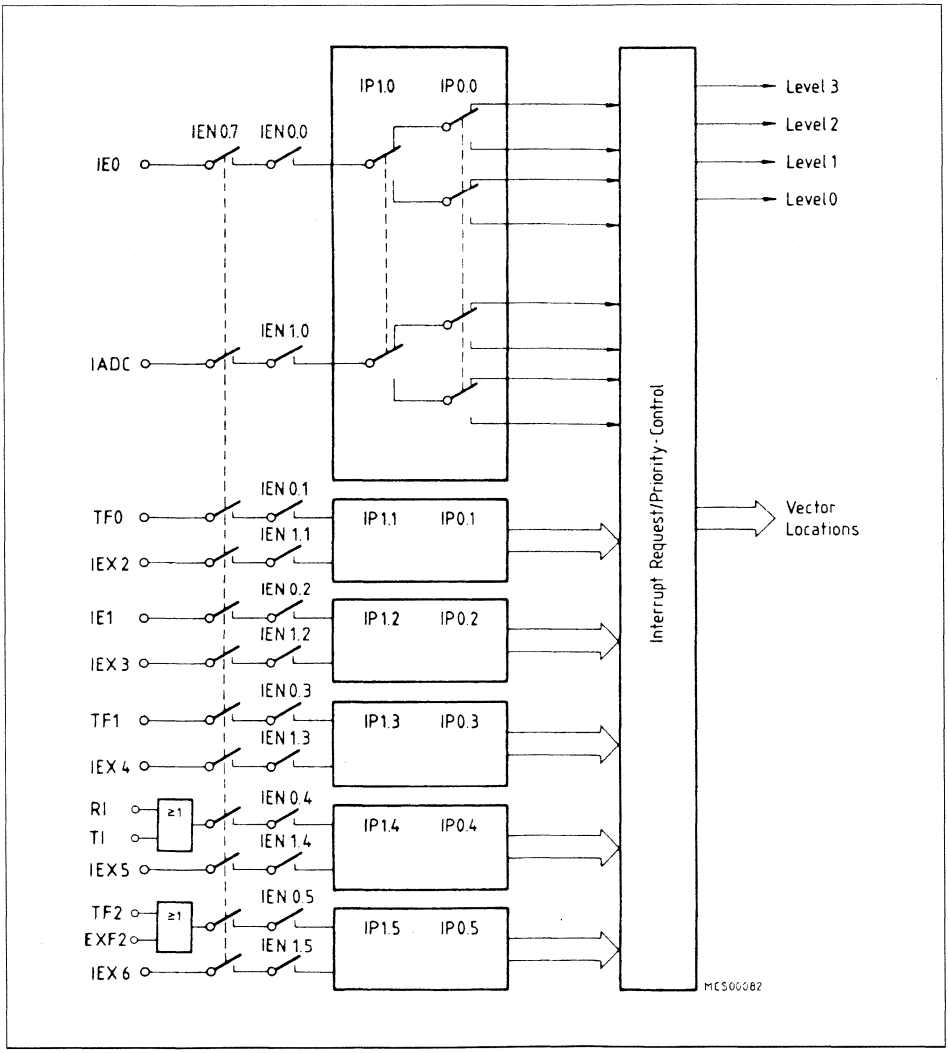


Figure 6
Interrupt Priority Level Structure

I/O Ports

The SAB 80C515A has six 8-bit I/O ports and one input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Ports 1, 3 and 4 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	$\overline{\text{INT6}}$/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external count or gate input
P3.0	RxD	Serial port's receiver data input (asynchronous) or data input /output (synchronous)
P3.1	TxD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	INT0	External interrupt 0 input, timer 0 gate control
P3.3	INT1	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe
P4.0	$\overline{\text{ADST}}$	A/D Converter, external start of conversion

The SAB 80C515A has one dual-purpose input port. The ANx lines of port 6 in the SAB 80C515 can individually be used as analog or digital inputs. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6. It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their V_{IL}/V_{IH} specifications. Furthermore, it is not possible to use port P6 as an output port. Special function register P6 is located at address 0DBH.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C515A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eight of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.
- The **Software Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current and is fully compatible to the Power Down Mode of the SAB 80C515.
- The **Hardware Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is new in the SAB 80C515A and is independent of the state of pin $\overline{\text{PE}}$/SWD (which enables only the software initiated power reduction modes).

Hardware Enable for Software controlled Power Saving Modes

A dedicated pin $\overline{\text{PE}}$/SWD of the SAB 80C515A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving moes can be activated by software. The watchdog timer can be started by software at any time.

When left unconnected, pin $\overline{\text{PE}}$/SWD is pulled high by a weak internall pull-up. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. The control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software Controlled Power Saving Modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C515A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{PSEN}$ hold at logic high levels (see table 5).

Software Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 5.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 5. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 5 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled. The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 ms).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset with oscillator watchdog status flag set.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal resetfunction.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode). function.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 5
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down
	internal ROM	external ROM	internal ROM	external ROM	Status
P0	Data	float	Data	float [1]	floating [1]
P1	Data alt outputs	Dat alt outputsa	Data last outputs	Data last outputs	
P2	Data	Address	Data	Data	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled
P5	Data alt output	Data alt output	Data last output	Data last output	input
P6	[1]	[1]	[1]	[1]	function
$\overline{EA}$					active input [2]
$\overline{PE}$/SWD					active input pull-up disabled [2]
XTAL1					active output
XTAL2					disabled input function [1]
$\overline{PSEN}$	high	high	low	low	floating output
ALE	high	high	low	low	
V_{AREF} V_{AGND}					active supply pins [3]
$\overline{RESET}$					active input must be high

[1] Applied voltage range at pin $V_{SS} \leq V_{IN} \leq V_{CC}$
[2] $V_{IN} = V_{SS}$ or $V_{IN} = V_{CC}$
[3] $V_{SS} \leq V_{IN} \leq V_{CC}$; $V_{AREF} \geq V_{AGND}$

Serial Interface

The SAB 80C515A has a full duplex and receive buffered serial interface. It is functionally identical with the serial interface of the SAB 8051.

Table 6 shows possible configurations and the according baud rates.

Table 6
Baud Rate Generation

	Mode		Mode 0		
8-Bit synchronous channel	Baudrate	f_{OSC} =12 MHz	1MHz		
		f_{OSC} =16 MHz	1.33 MHz		
		f_{OSC} =18 MHz	1.5 MHz		
	derived from		f_{OSC}		
	Mode		**Mode 1**		
8-Bit UART	Baudrate	f_{OSC} =12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud
		f_{OSC} =16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud
		f_{OSC} =18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**	
9-Bit UART	Baudrate	f_{OSC} =12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud –75 kBaud
		f_{OSC}=16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud
		f_{OSC} =18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud – 562.5 kBaud
	derived from		$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator

The Serial Interface can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D. T × D outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register SCON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in SCON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface

Variable baud rates for modes 1 and 3 of serial interface can be derived from either timer 1 or a new dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{SMOD} * f_{OSC}}{64*(2^{10}\text{-SREL})}$$

The default value after reset in the reload registers SRELL and SRELH provides a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C515.

Fail Safe Units

The SAB 80C515A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

- a programmable watchdog timer (WDT), with variable time-out period from 512 µs up to appr. 1.1 s @12 MHz. Upward compatible to SAB 80C515 watchdog timer.
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state, in case the on-chip oscillator fails; it also controls the restart from the Hardware Power Down Mode and provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C515A then starts program execution with the WDT running. Since pin $\overline{PE}$/SWD is only sampled during Reset, the WDT cannot be started externally during normal operation.

Software initialization is done by setting bit SWDT in SFR IEN1.

A refresh of the watchdog timer is done by setting bits WDT (SFR IEN0) and SWDT consecutively. This double instruction sequence has been implemented to increase system security.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS (SFR IP0) is set. This flag can also be cleared by software.

Figure 7 shows the block diagram of the programmable Watchdog Timer.

Oscillator Watchdog

The unit serves three functions:

- Monitoring of the on-chip oscillator's function.
  The watchdog monitors the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- Restart from the Hardware Power Down Mode.
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.
- Fast internal reset after power-on.
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

Figure 8 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the frequency comparator.

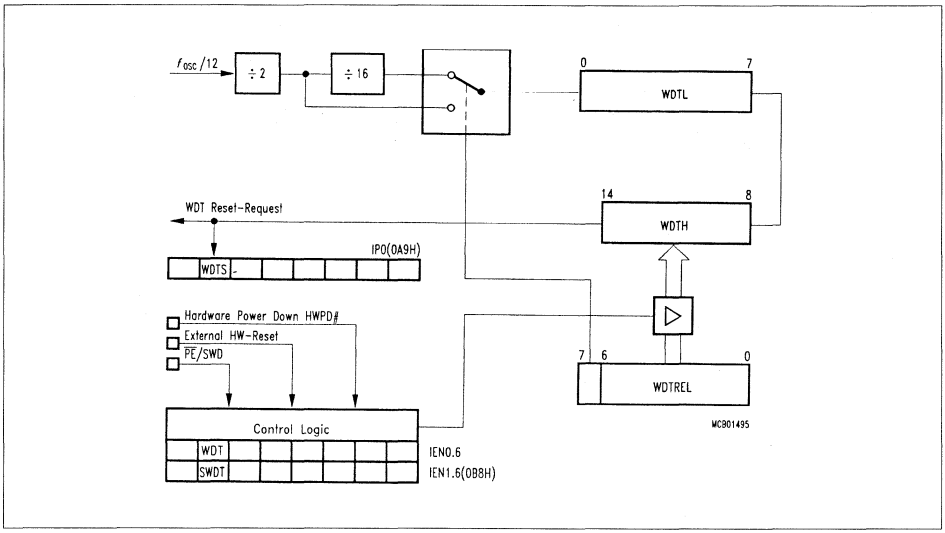


Figure 7
Block Diagram of the Programmable Watchdog Timer

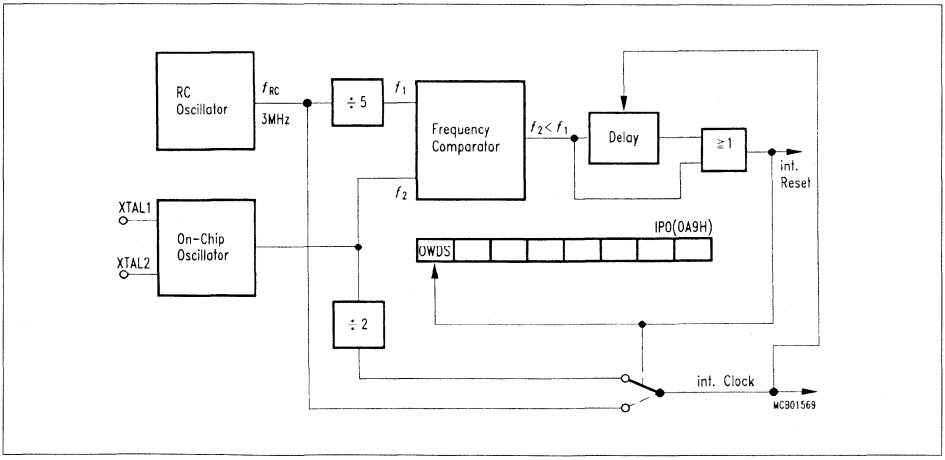


Figure 8
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C515A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C515) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C515A the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 ms). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C515A / 83C515A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias ..... – 40 to 110° C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC}+0.5 V
Input current on any pin during overload condition ..... –10mA to +10mA
Absolute sum of all input currents during overload condition 100mA
Power dissipation ..... 1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C515A
T_A = – 40 to 85 °C for the SAB 80C515A-T3
T_A = – 40 to 110 °C for the SAB 80C515A-T4

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (exept $\overline{EA}$,$\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} –0.1	V	–
Input low voltage $\overline{EA}$	V_{IL1}	– 0.5	0.2 V_{CC} –0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} +0.1	V	–
Input high voltage (exept $\overline{RESET}$, XTAL2 and $\overline{HWPD}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC}+ 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC}+ 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC}+ 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5)	V_{OL}	–	0.45	V	I_{OL} =1.6 mA [1]
Output low voltage (ports 0, ALE, $\overline{RESET}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, (ports1, 2, 3, 4, 5)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode,- ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3, 4, 5)	I_{IL}	– 10	– 70	µA	V_{IN} = 2 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	ITL	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, P6, $\overline{HWPD}$)	I_{LI}	– –	± 100 ± 150	nA nA	0.45 < V_{IN} < V_{CC} 0.45 < V_{IN} < V_{CC} T_A > 100°C
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
Input low current ($\overline{XTAL2}$)	I_{IL3}	–	–15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25°C
Power-supply current: Active mode, 12 MHz [7] Active mode, 18 MHz [7] Idle mode, 12 MHz [7] Idle mode, 18 MHz [7] Slow down mode, 12 MHz Slow down mode, 18 MHz Power Down Mode	 – I_{CC} – I_{CC} – I_{CC} – I_{CC} – I_{CC} – I_{CC} – I_{PD}	 – – – – – – –	 26 35 11.8 14.2 9 10 50	 mA mA mA mA mA mA µA	 V_{CC} = 5 V [4] V_{CC} = 5 V [4] V_{CC} = 5 V [5] V_{CC} = 5 V [5] V_{CC} = 5 V [6] V_{CC} = 5 V [6] V_{CC} = 2... 5.5 V [3]

Notes see page 206.

Notes for page 205:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Software Power Down Mode) is measured under following conditions:
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port0 = Port6 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = V_{SS}; $\overline{HWPD}$ = V_{CC}; V_{AGND} = V_{SS}; V_{ARef} = V_{CC}; all other pins are disconnected.
I_{PD} (Hardware Power Down Mode): independent of any particular pin connection.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; XTAL1 = N.C.; $\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS};
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

7) I_{CC} Max at other frequencies is given by:
active mode: I_{CC} (max) = 1.5 * f_{OSC} + 8
idle mode: I_{CC} (max)= 0.4 * f_{OSC} + 7
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5
T_A = – 40 to 85 ° C for the SAB 80C515A-T3/83C515A-5-T3
T_A = – 40 to 110 °C for the SAB 80C515A-T4/83C515A-5-T4

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			4 t_{CY} [1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
V_{AREF} supply current	I_{REF}		± 20		µA	

[1] $t_{CY} = (8*2^{ADCL}) / f_{OSC}$; ($t_{CY} = 1/f_{ADC}$; $f_{ADC} = f_{OSC}/(8*2^{ADCL})$)
[2] This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
[3] This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.

AC Characteristics

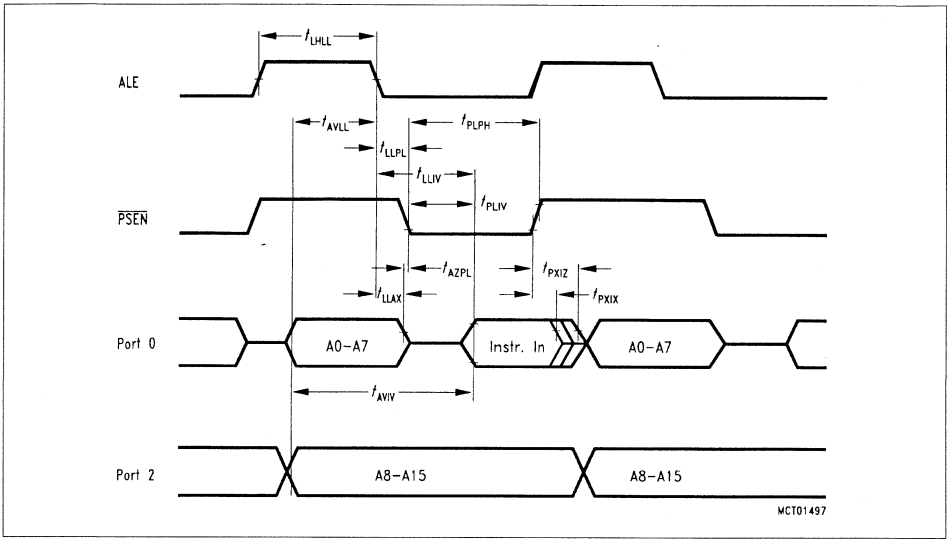
V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5
T_A = – 40 to 85 °C for the SAB 80C515A-T3/83C515A-5-T3
T_A = – 40 to110 °C for the SAB 80C515A-T4/83C515A-5-T4
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 1 MHz to 18 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	71	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	26	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	26	–	$t_{CLCL} - 30$	–	ns
ALE to valid instruction in	t_{LLIV}	–	122	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	92	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	46	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	48	–	$t_{CLCL} - 8$	–	ns
Address to valid instruction in	t_{AVIV}	–	218	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

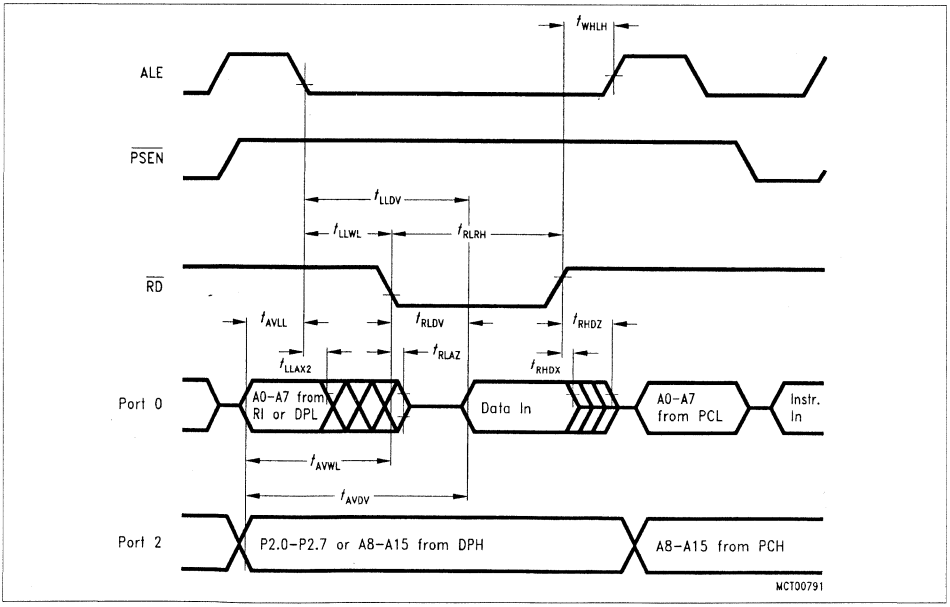
*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

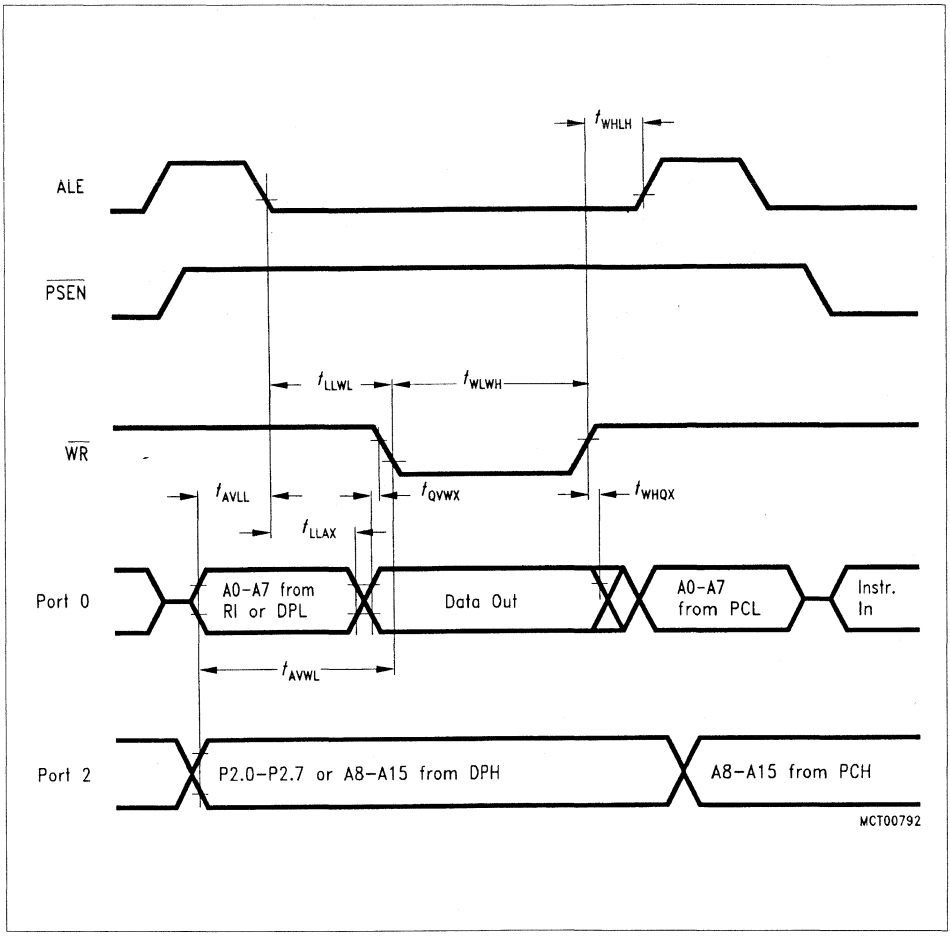
Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 1 MHz to 18 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



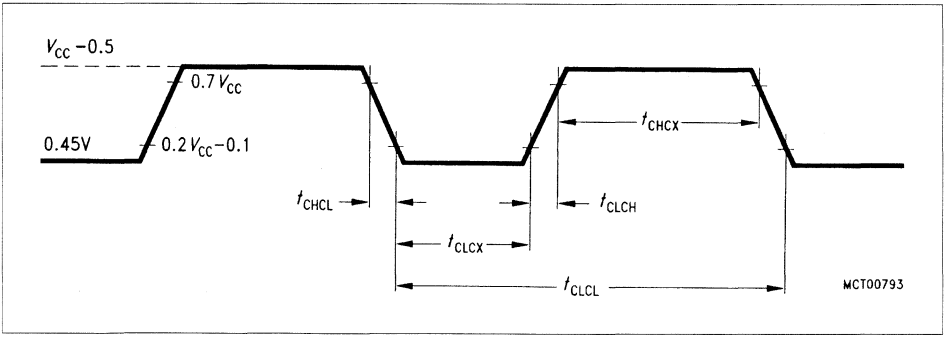
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

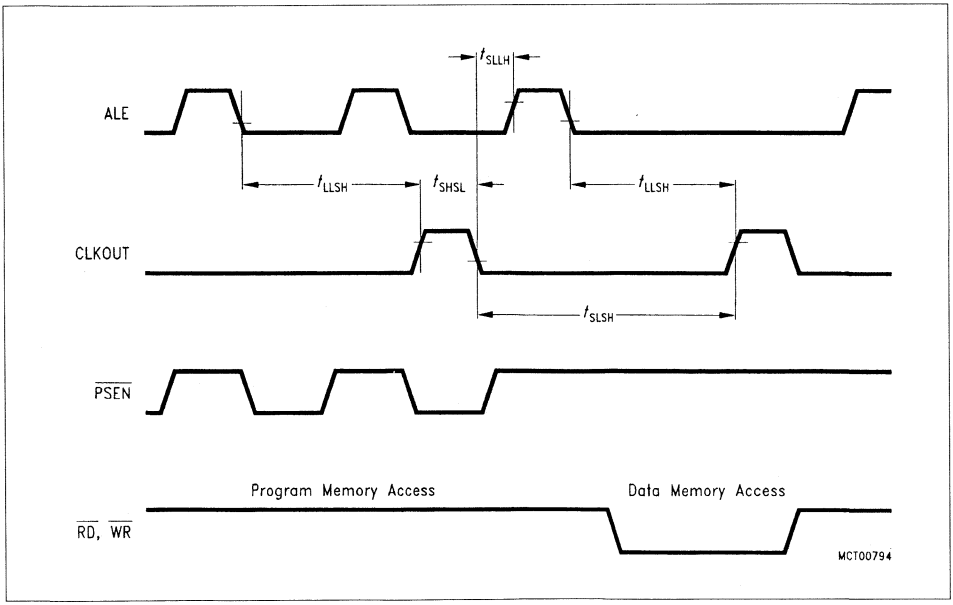
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1 MHz to 18 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	1000	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CLCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	1	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 1 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	$7\,t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	71	–	$2\,t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	516	–	$10\,t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



System Clock Timing

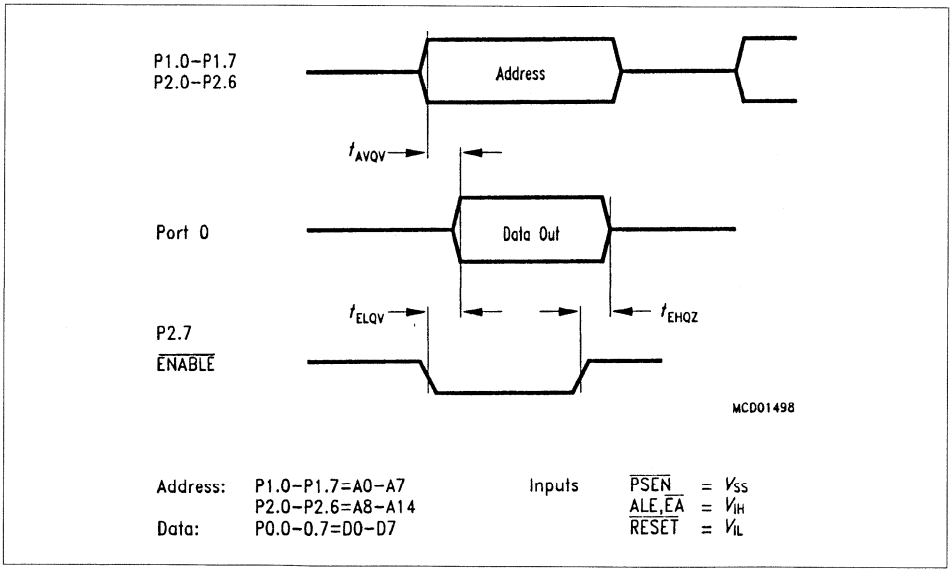
ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V + 10\%, -15\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	

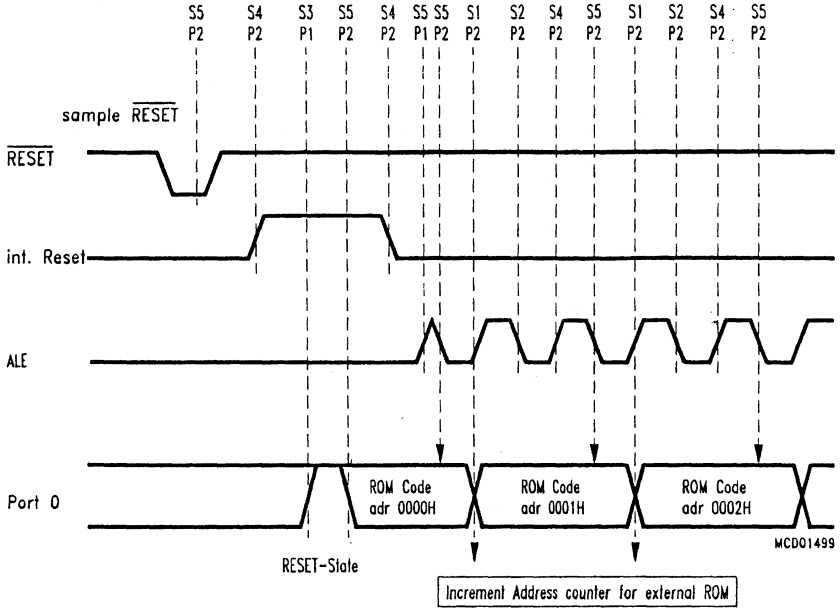
ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



ROM Verification Mode 1

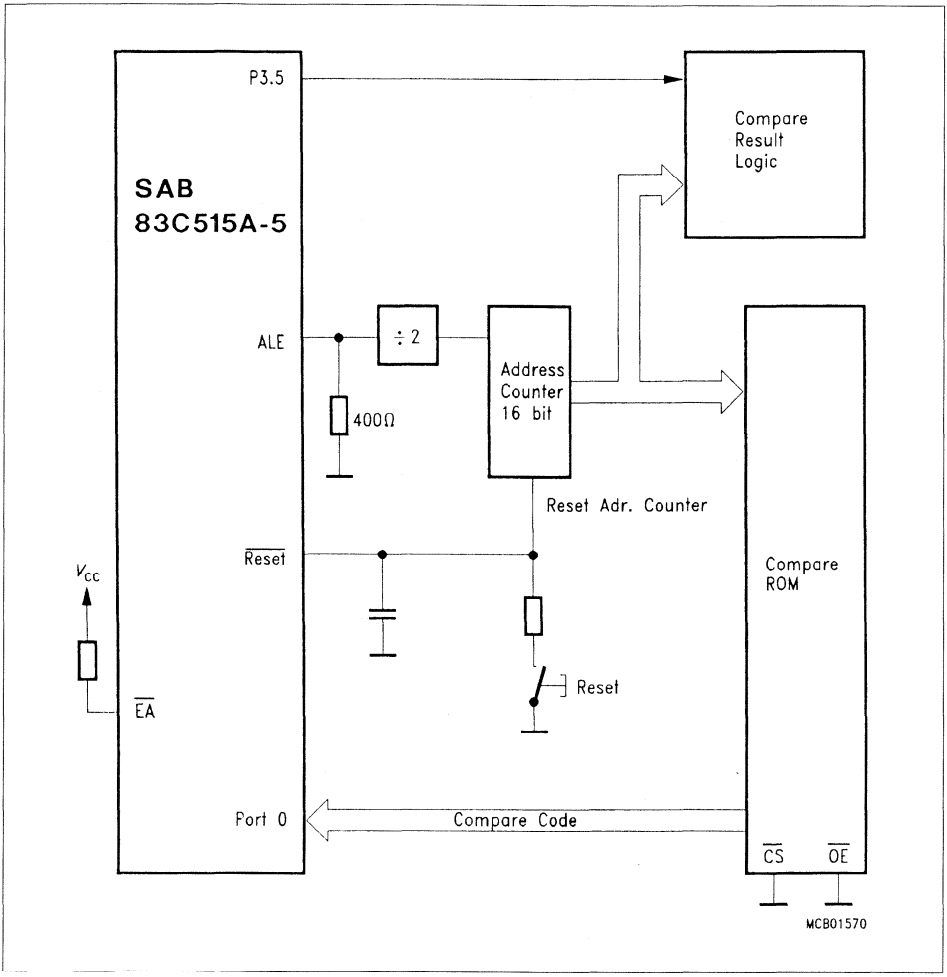
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



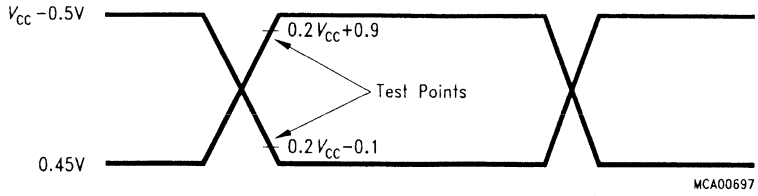
Inputs $\overline{EA}= V_{IH}$
ALE forced to low level by a weak pull down resistor (approx.400Ω),
durind $\overline{RESET}$ activ ROM-Code: Port 0=D0-D7

Outputs Port 3.5 shows all 1024 cycles low level for one cycle
when compared ROM-Code was not allright

ROM Verification Mode 2

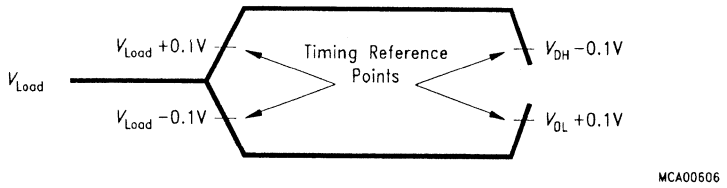


Application Example for Verifying the Internal ROM with ROM Verify Mode 2



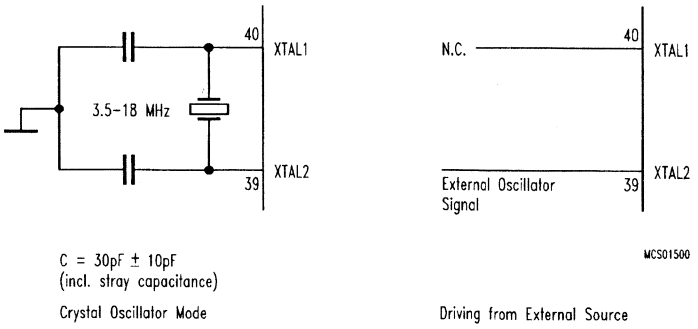
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



Recommended Oscillator Circuits

SIEMENS

High-Performance
8-Bit CMOS Single-Chip Microcontroller

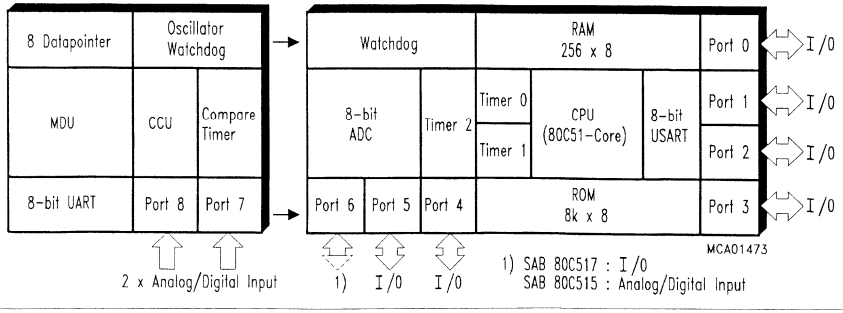
SAB 80C517/80C537

Advanced Information

SAB 80C517	Microcontroller with factory mask-programmable ROM
SAB 80C537	Microcontroller for external ROM

- Versions for 12 MHz and 16 MHz operating frequency
- 8 K × 8 ROM (SAB 80C517 only)
- 256 × 8 on-chip RAM
- Superset of SAB 80C51 architecture:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  256 directly addressable bits
  Boolean processor
  64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output
  channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit 2 multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Fourteen interrupt vectors, four priority levels selectable
- 8-bit A/D converter with 12 multiplexed inputs and programmable ref. voltages
- Two full duplex serial interfaces
- Fully upward compatible with SAB 80C515
- Extended power saving modes
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70 °C
  – 40 to 85 °C
- Plastic packages: P-LCC-84, P-MQFP-100-2

SAB 80C517/80C537

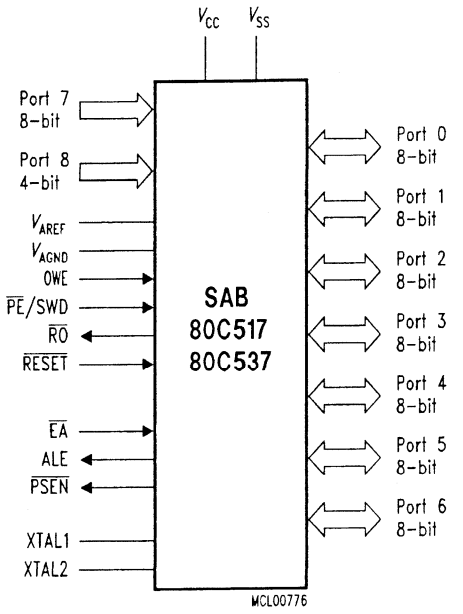


The SAB 80C517/80C537 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

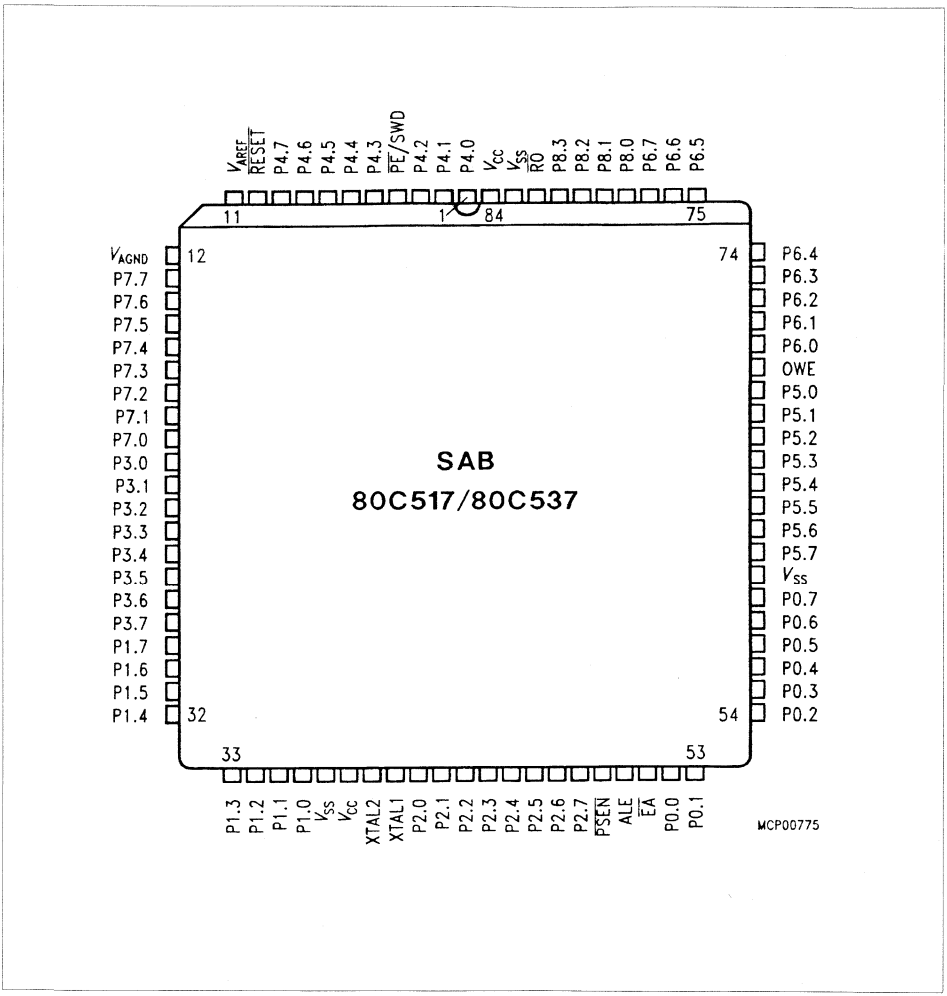
While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C517 is expanded in its arithmetic capabilities, "fail-safe" characteristics, analog signal processing and timer capabilities. The SAB 80C537 is identical with the SAB 80C517 except that it lacks the on-chip program memory. The SAB 80C517/SAB 80C537 is supplied in a 84 pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad metric flat package (P-MQFP-100-2).

Ordering Information

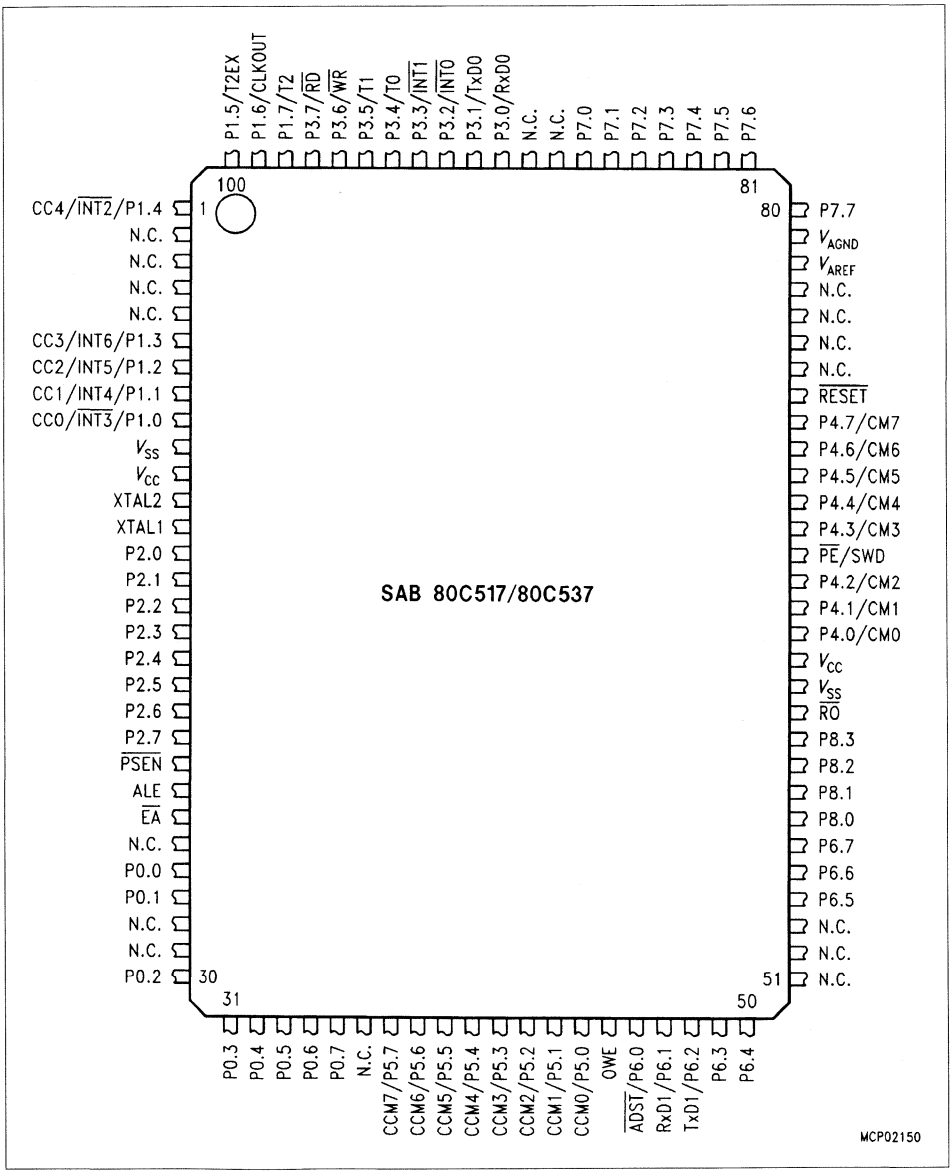
Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C517-N	Q67120-C397	P-LCC-84	with factory mask-programmable ROM,12 MHz
SAB 80C517-M	TBD	P-MQFP-100-2	
SAB 80C537-N	Q67120-C452	P-LCC-84	for external memory, 12 MHz
SAB 80C537-M	TBD	P-MQFP-100-2	
SAB 80C517-N-T40/85	Q67120-C483	P-LCC-84	with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to 85 °C
SAB 80C517-M-T40/85	TBD	P-MQFP-100-2	
SAB 80C537-N-T40/85	Q67120-C484	P-LCC-84	for external ROM, 12 MHz, ext. temperature – 40 to 85 °C
SAB 80C537-M-T40/85	TBD	P-MQFP-100-2	
SAB 80C517-N16	Q67120-C723	P-LCC-84	with mask-programmable ROM,16 MHz ext. temperature – 40 to 110 °C
SAB 80C517-M16	TBD	P-MQFP-100-2	
SAB 80C537-N16	Q67120-C722	P-LCC-84	for external memory, 16 MHz
SAB 80C537-M16	TBD	P-MQFP-100-2	
SAB 80C517-N16-T40/85	Q67120-C724	P-LCC-84	with mask-programmable ROM, 16 MHz ext. temperature – 40 to 85 °C
SAB 80C517-16-N-T40/85	Q67120-C725	P-LCC-84	with factory mask-programmable ROM,12 MHz



Logic Symbol



Pin Configuration
(P-LCC-84)



Pin Configuration
(P-MQFP-100-2)

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P4.0 – P4.7	1– 3, 5 – 9	64 - 66, 68 - 72	I/O	**Port 4** is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
$\overline{PE}$/SWD	4	67	I	**$\overline{PE}$/SWD Power saving modes enable/Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{RESET}}$	10	73	I	$\overline{\text{RESET}}$ A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	78		**Reference voltage** for the A/D converter.
V_{AGND}	12	79		**Reference ground** for the A/D converter.
P7.7 -P7.0	13 - 20	80 - 87	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P3.0 - P3.7	21 - 28	90 - 97	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D0 (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D0 (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control – $\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P1.7 - P1.0	29 - 36	98 - 100, 1, 6 - 9	I/O	**Port 1** is a bidirectional I/O port with inter-nal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC character-istics) because of the internal pull-up resistors. It is used for the low order address byte during program verifi-cation. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): $\overline{\text{interrupt 3 input}}$/ compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output /capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output /capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output /capture 3 input – $\overline{\text{INT2}}$/CC4 (P1.4): $\overline{\text{interrupt 2 input}}$ / compare 4 output /capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
XTAL2	39	12	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	13	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is devided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	41 - 48	14 - 21	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{PSEN}$	49	22	O	The **Program Store Enable** output is a control signal that en-ables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal pro-gram execution.
ALE	50	23	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscil-lator periodes except during an exter-nal data memory access
$\overline{EA}$	51	24	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM when the PC is less than 8192. When held at low level, the SAB 80C517 fet-ches all instructions from external pro-gram memory. For the SAB 80C537 this pin must be tied low
P0.0 - P0.7	52 - 59	26 - 27, 30 - 35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impe-dance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also out-puts the code bytes during program verifica-tion in the SAB 83C517. External pull-up resistors are required during program verification.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P5.7 - P5.0	61 - 68	37 - 44	I/O	**Port 5** is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 (P5.0): concurrent compare 0 – CCM1 (P5.1): concurrent compare 1 – CCM2 (P5.2): concurrent compare 2 – CCM3 (P5.3): concurrent compare 3 – CCM4(P5.4): concurrent compare 4 – CCM5 (P5.5): concurrent compare 5 – CCM6 (P5.6): concurrent compare 6 – CCM7(P5.7): concurrent compare 7
OWE	69	45	I	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P6.0 - P6.7	70 - 77	46 - 50, 54 - 56	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: – $\overline{\text{ADST}}$ (P6.0): external A/D converter start pin – R × D1 (P6.1): receiver data input of serial interface 1 – T × D1 (P6.2): transmitter data output of serial interface 1
P8.0 - P8.3	78 - 81	57 - 60	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{RO}$	82	61	O	**$\overline{\text{Reset Output}}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low.
V_{SS}	37,60, 83	10, 62	–	**Circuit ground potential**
V_{CC}	38,84	11, 63	–	**Supply Terminal** for all operating modes
N.C.	–	2 - 5, 25, 28 - 29, 36, 51 - 53, 74 - 77, 88 - 89	–	Not connected

* I = Input
O = Output

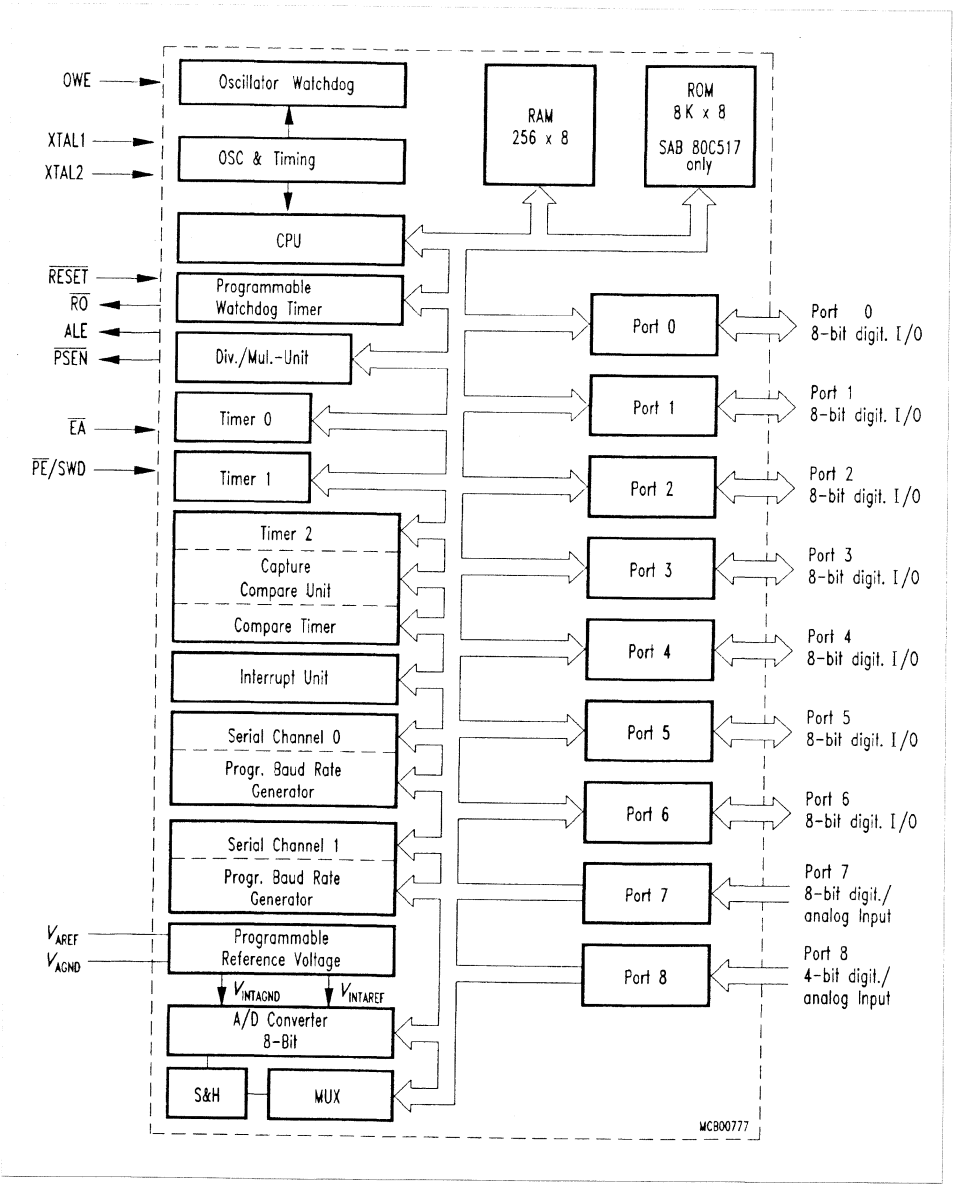


Figure 1
Block Diagram

Functional Description

The SAB 80C517 is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being a significantly enhanced SAB 80C515. The SAB 80C517 is therefore 100 % compatible with code written for the SAB 80C515.

CPU

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517 is optimized for control applications. With a 12 MHz crystal, 58 % of the instructions execute in 1 µs.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517 has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

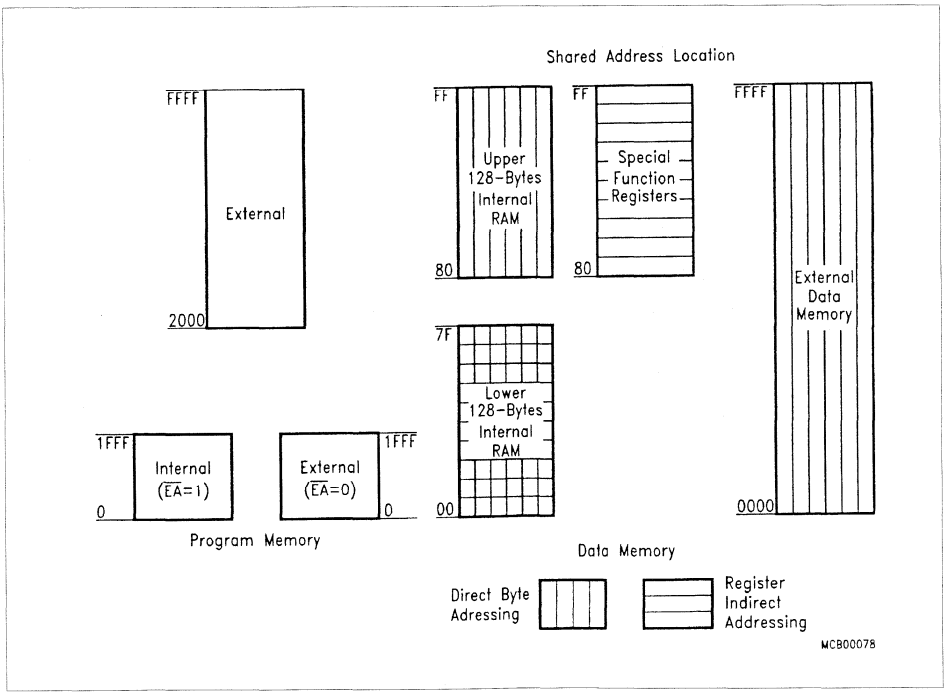


Figure 2
Memory Mapping

Program Memory

The SAB 80C517 has 8 KByte of on-chip ROM, while the SAB 80C537 has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ controls whether program fetches below address 2000H are done from internal or external memory.

Data Memory

The data memory space consists of an internal and an external memory space.

External Data Memory

Up to 64 KByte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions utilizing registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers.

Multiple Datapointers

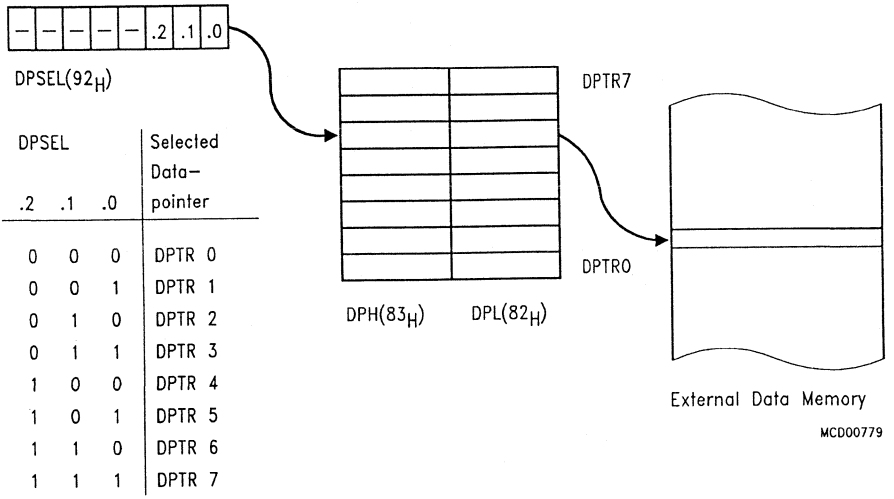
As a functional enhancement to standard 8051 controllers, the SAB 80C517 contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointers is done in special function register DPSEL (data pointer select,
addr. 92H). Figure 3 illustrates the addressing mechanism.

Internal Data Memory

The internal data memory is divided into three physically distinct blocks:

- the lower 128 bytes of RAM including four banks of eight registers each
- the upper 128 byte of RAM
- the 128 byte special function register area.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes. The stack can be located anywhere in the internal data memory.



DPSEL .2	DPSEL .1	DPSEL .0	Selected Data-pointer
0	0	0	DPTR 0
0	0	1	DPTR 1
0	1	0	DPTR 2
0	1	1	DPTR 3
1	0	0	DPTR 4
1	0	1	DPTR 5
1	1	0	DPTR 6
1	1	1	DPTR 7

Figure 3
Addressing of External Data Memory

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1. In this table they are organized in groups which refer to the functional blocks of the SAB 80C517. Block names and symbols are listed in alphabetical order.

Table 1
Special Function Register

Block	Symbol	Name	Address	Contents after Reset
CPU	**ACC**	**Accumulator**	**$0E0_H$** [1]	**00_H**
	B	**B-Register**	**$0F0_H$** [1]	**00_H**
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	XXXX.X000B [3]
	PSW	**Program Status Word**	**$0D0_H$** [1]	**00_H**
	SP	**Register**		
		Stack Pointer	81_H	07_H
A/D-Converter	**ADCON0**	**A/D Converter Control**	**$0D8_H$** [1]	**00_H**
	ADCON1	**Register 0**		
	ADDAT	A/D Converter Control Register 1	$0DC_H$	XXXX.0000B [3]
	DAPR	A/D Converter Data Register	$0D9_H$	00_H
		D/AConverter Program Register	$0DA_H$	00_H
Interrupt System	**IEN0**	**Interrupt Enable Register 0**	**$0A8_H$** [1]	**00_H**
	CTCON [2]	Com. Timer Control Register	$0E1_H$	0XXX.0000B [3]
	IEN1	**Interrupt Enable Register 1**	**$0B8_H$** [1]	00_H
	IEN2	Interrupt Enable Register 2	$9A_H$	XXXX.00X0B [3]
	IP0	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1	Interrupt Priority Register 1	$0B9_H$	XX00.0000B [3]
	IRCON	**Interrupt Request Control**	**$0C0_H$** [1]	**00_H**
	TCON [2]	**Register**		
	T2CON [2]	**Timer Control Register**	**88_H** [1]	**00_H**
		Timer 2 Control Register	**$0C8_H$** [1]	**00_H**

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Block	Symbol	Name	Address	Contents after Reset
MUL/DIV Unit	ARCON	Arithmetic Control Register	$0EF_H$	0XXX.XXXXB [3]
	MD0	Multiplication/Division Register 0	$0E9_H$	XX_H [3]
	MD1	Multiplication/Division Register 1	$0EA_H$	XX_H [3]
	MD2	Multiplication/Division Register 2	$0EB_H$	XX_H [3]
	MD3	Multiplication/Division Register 3	$0EC_H$	XX_H [3]
	MD4	Multiplication/Division Register 4	$0ED_H$	XX_H [3]
	MD5	Multiplication/Division Register 5	$0EE_H$	XX_H [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CC4EN	Comp./Capture Enable 4 Reg.	$0C9_H$	X000.0000B [3]
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCH4	Comp./Capture Reg. 4, High Byte	$0CF_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CCL4	Comp./Capture Reg. 4, Low Byte	$0CE_H$	00_H
	CMEN	Compare Enable Register	$0F6_H$	00_H
	CMH0	Compare Register 0, High Byte	$0D3_H$	00_H
	CMH1	Compare Register 1, High Byte	$0D5_H$	00_H
	CMH2	Compare Register 2, High Byte	$0D7_H$	00_H
	CMH3	Compare Register 3, High Byte	$0E3_H$	00_H
	CMH4	Compare Register 4, High Byte	$0E5_H$	00_H
	CMH5	Compare Register 5, High Byte	$0E7_H$	00_H
	CMH6	Compare Register 6, High Byte	$0F3_H$	00_H
	CMH7	Compare Register 7, High Byte	$0F5_H$	00_H
	CML0	Compare Register 0, Low Byte	$0D2_H$	00_H
	CML1	Compare Register 1, Low Byte	$0D4_H$	00_H
	CML2	Compare Register 2, Low Byte	$0D6_H$	00_H
	CML3	Compare Register 3, Low Byte	$0E2_H$	00_H
	CML4	Compare Register 4, Low Byte	$0E4_H$	00_H
	CML5	Compare Register 5, Low Byte	$0E6_H$	00_H
	CML6	Compare Register 6, Low Byte	$0F2_H$	00_H
	CML7	Compare Register 7, Low Byte	$0F4_H$	00_H
	CMSEL	Compare Input Select	$0F7_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	CTCON	Com. Timer Control Reg.	$0E1_H$	0XXX.0000B [3]
	CTRELH	Com. Timer Rel. Reg., High Byte	$0DF_H$	00_H
	CTRELL	Com. Timer Rel. Reg., Low Byte	$0DE_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON	**Timer 2 Control Register**	**$0C8_H$** [1]	**00_H**

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	**P0**	**Port 0**	**80_H** [1]	**FF_H**
	P1	**Port 1**	**90_H** [1]	**FF_H**
	P2	**Port 2**	**$0A0_H$** [1]	**FF_H**
	P3	**Port 3**	**$0B0_H$** [1]	**FF_H**
	P4	**Port 4**	**$0E8_H$** [1]	**FF_H**
	P5	**Port 5**	**$0F8_H$** [1]	**FF_H**
	P6	Port 6,	$0FA_H$	FF_H
	P7	Port 7, Analog/Digital Input	$0DB_H$	XX_H [3]
	P8	Port 8, Analog/Digital Input, 4-bit	$0DD_H$	XX_H [3]
Pow.Sav. Modes	PCON	Power Control Register	87_H	00_H
Serial Channels	**ADCON0** [2]	**A/D Converter Control Reg.**	**$0D8_H$** [1]	**00_H**
	PCON [2]	Power Control Register	87_H	00_H
	S0BUF	Serial Channel 0 Buffer Reg.	99_H	XX_H [3]
	S0CON	**Serial Channel 0 Control Reg.**	**98_H** [1]	**00_H**
	S1BUF	Serial Channel 1 Buffer Reg.,	$9C_H$	XX_H [3]
	S1CON	Serial Channel 1 Control Reg.	$9B_H$	0X00.0000B [3]
	S1REL	Serial Channel 1 Reload Reg.	$9D_H$	00_H
Timer 0/ Timer 1	**TCON**	**Timer Control Register**	**88_H** [1]	**00_H**
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	**IEN0** [2]	**Interrupt Enable Register 0**	**$0A8_H$** [1]	**00_H**
	IEN1 [2]	**Interrupt Enable Register 1**	**$0B8_H$** [1]	**00_H**
	IP0 [2]	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1 [2]	Interrupt Priority Register 1	$0B9_H$	XX00.0000B [3]
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

A/D Converter

The SAB 80C517 contains an 8-bit A/D Converter with 12 multiplexed input channels which uses the successive approximation method. It takes 7 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 13 machine cycles (13 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter are both programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range (see table 2).

Table 2
Adjustable Internal Reference Voltages

Step	DAPR (.3-.0) DAPR (.7-.4)	$V_{IntAGND}$	$V_{IntAREF}$
0	0000	0.0	5.0
1	0001	0.3125	–
2	0010	0.625	–
3	0011	0.9375	–
4	0100	1.25	1.25
5	0101	1.5625	1.5625
6	0110	1.875	1.875
7	0111	2.1875	2.1875
8	1000	2.5	2.5
9	1001	2.8125	2.8125
10	1010	3.125	3.125
11	1011	3.4375	3.4375
12	1100	3.75	3.75
13	1101	–	4.0625
14	1110	–	4.375
15	1111	–	4.68754

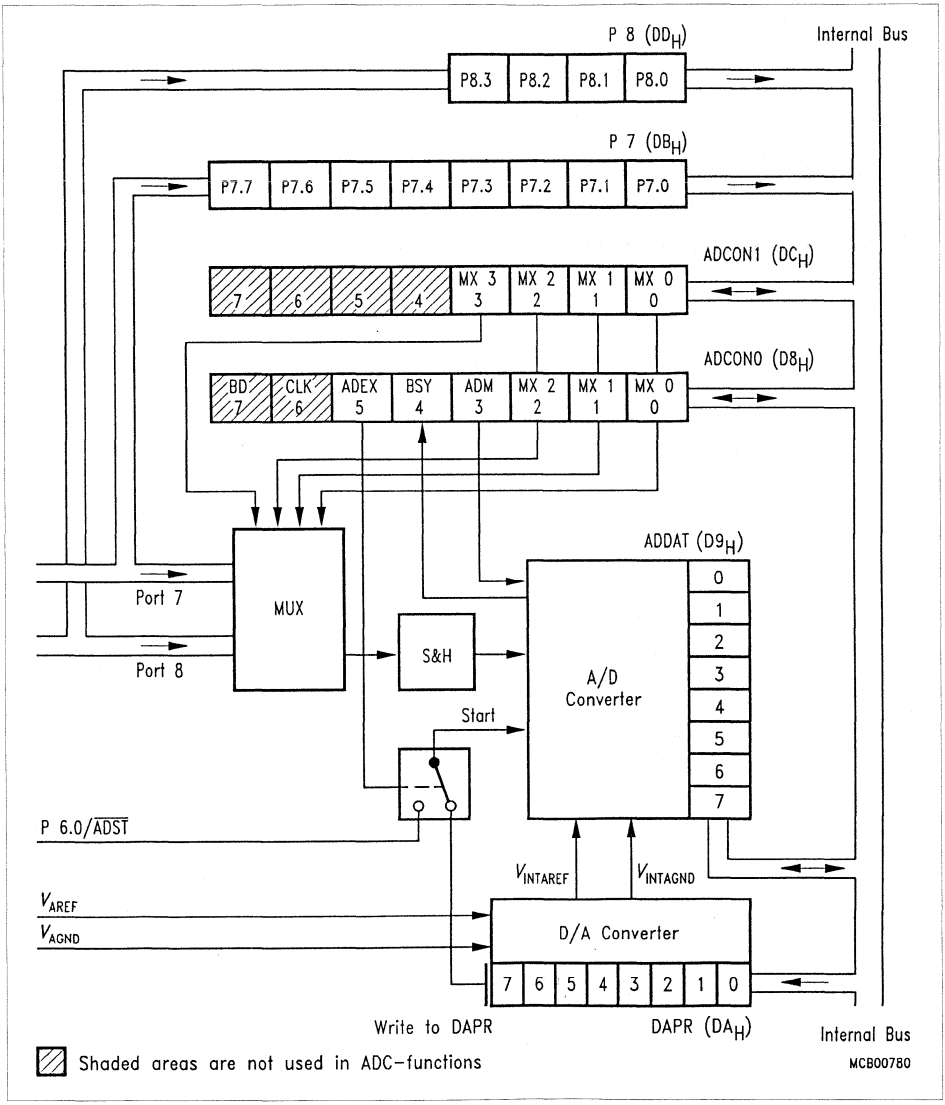


Figure 4
Block Diagram A/D Converter

Compare/Capture Unit (CCU)

The compare capture unit is a complex timer/register array for applications that require high speed I/O, pulse width modulation and more timer/counter capabilities. The CCU contains

- one 16-bit timer/counter **(timer 2)** with 2-bit prescaler, reload capability and a max.clock frequency of $f_{OSC}/12$ (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of $f_{OSC}/2$ (6 MHz with a 12 MHz crystal).
- thirteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- seven interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers and the compare/reload/capture register are always connected to timer 2. Dependent on the register type and the assigned timer two compare modes can be selected. Table 3 illustrates possible combinations and the corresponding output lines.

Table 3
CU Compare Configuration

Assigned Timer	DAPR (.3-.0) DAPR (.7-.4)	$V_{IntAGND}$	$V_{IntAREF}$
Timer 2	CRCH/CRCL	P1.0/$\overline{INT3}$/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/$\overline{INT6}$/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/$\overline{INT2}$/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	CM0H/CM0L	P4.0/CM0	Comp. mode 1
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 1
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with add. latches)
	:	:	:
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with add. latches)

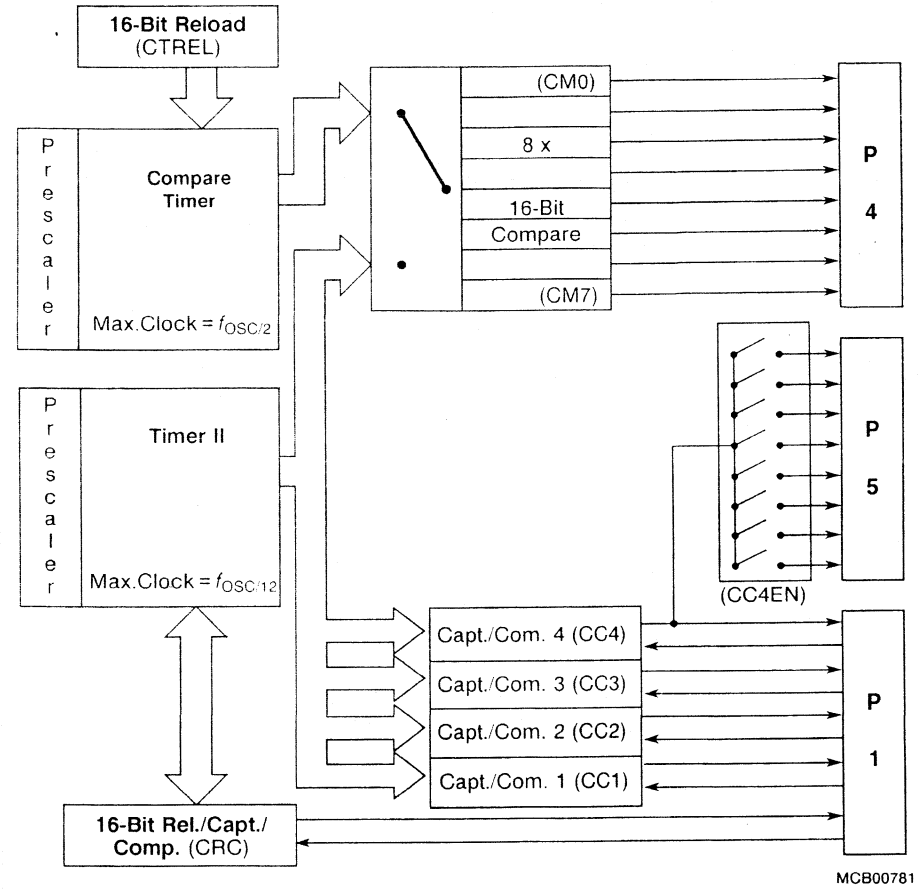


Figure 5
Block Diagram of the Compare/Capture Unit

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when the timer overflows.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal doesn't affect the compare-output.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which also can request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

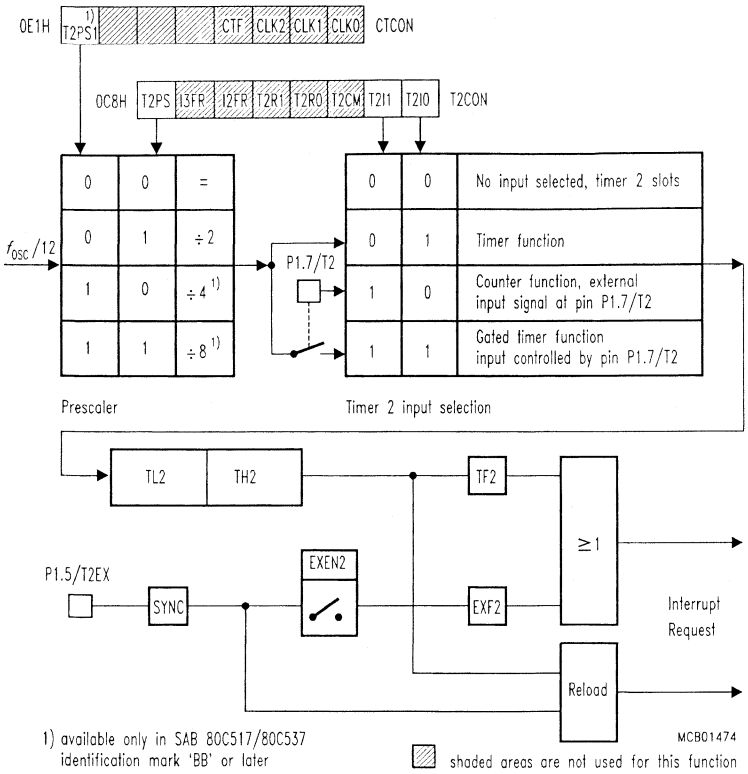


Figure 6
Block Diagram of Timer 2

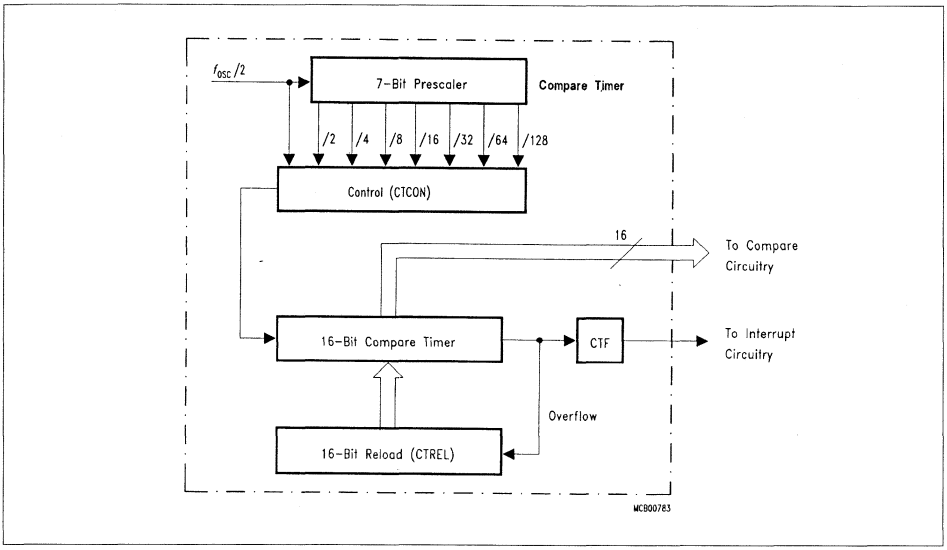


Figure 7
Block Diagram of the Compare Timer

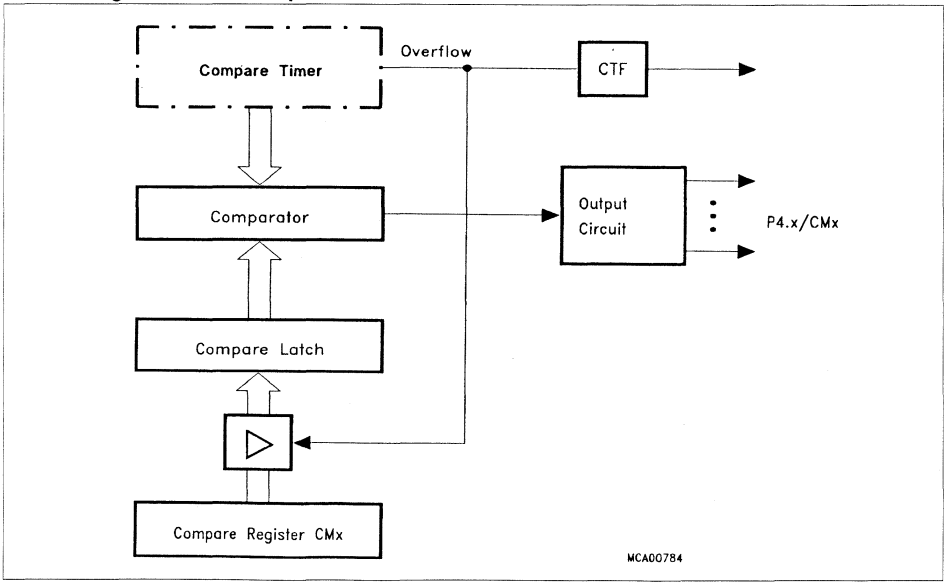


Figure 8
Compare-Mode 0 with Registers CM0 to CM7

Interrupt Structure

The SAB 80C517 has 14 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Source and Vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Source
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 overflow
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 overflow
RI0/TI0	0023_H	Serial channel 0
TF2/EXF2	$002B_H$	Timer 2 overflow/ext. reload
IADC	0043_H	A/D converter
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6
RI1/TI1	0083_H	Serial channel 1
CTF	$009B_H$	Compare timer overflow

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

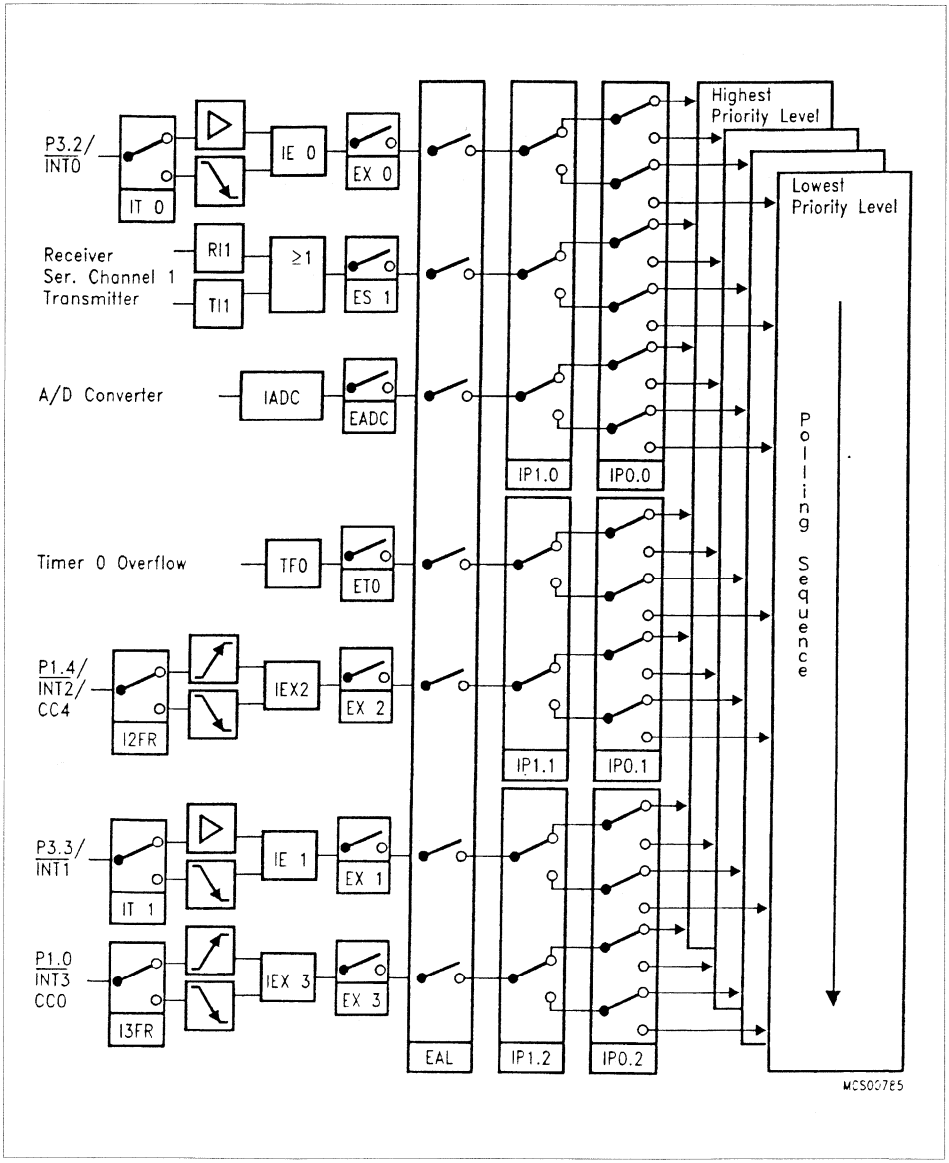


Figure 9
Interrupt Structure

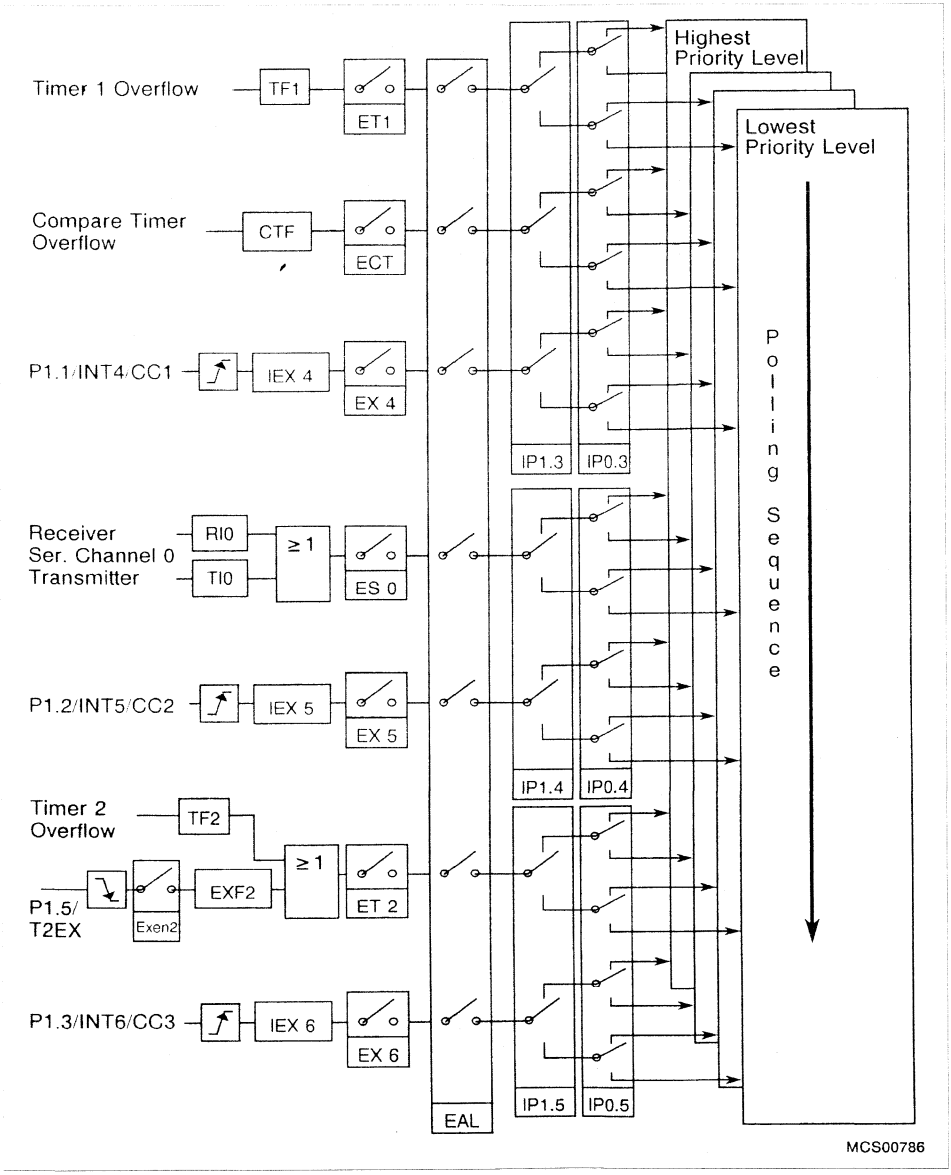


Figure 9 (cont'd)
Interrupt Structure

Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operations.

Operation	Result	Remainder	Execution Time
32-bit/16-bit 16-bit/16-bit	32-bit 16-bit	16-bit 16-bit	6 t_{cy} [1]) 4 t_{cy}
16-bit * 16-bit	32-bit	–	4 t_{cy}
32-bit normalize	–	–	6 t_{cy} [2])
32-bit shift left/right	–	–	6 t_{cy} [2])

[1]) 1 t_{cy} = 1 µs @ 12 MHz oscillator frequency.
[2]) The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:

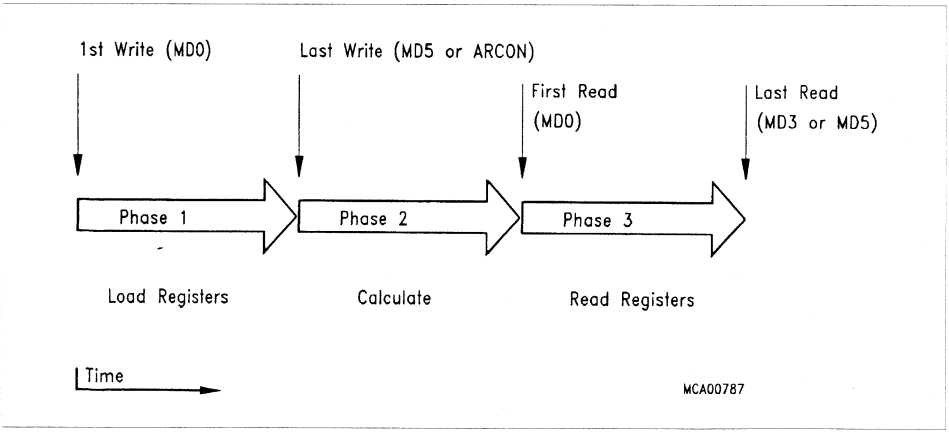


Figure 10
Operation of the MDU

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

Table 5
Performing a MDU-Calculation

Operation	32-Bit/16-Bit		16-Bit/16-Bit		16-Bit * 16-Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'end	MD4	M'orL
	MD2	D'end	MD2	D'end	MD1	M'andH
	MD3	D'endH	MD3	D'endH	MD5	M'orH
	MD4	D'orL	MD4	D'orL		
Last Write	MD5	D'orH	MD5	D'orH		
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	Quo	MD1	Pr
	MD2	Quo	MD2	Quo	MD2	Pr
	MD3	QuoH	MD3	QuoH	MD3	PrH
	MD4	RemL	MD4	RemL		
Last Read	MD5	RemH	MD5	RemH		

Table 6
Shift Operation with the CCU

Operation	Normalize, Shift Left, Shift Right	
First Write	MD0	least significant byte
	MD1	
	MD2	
	MD3	most significant byte
Last Write	ARCON	start of conversion
First Read	MD0	least significant byte
	MD1	
	MD2	
Last Read	MD3	most significant byte

Abbreviations

D'end : Dividend, 1st operand of division
D'or : Divisor, 2nd operand of division
M'and : Multiplicand, 1st operand of multiplication
M'or : Multiplicator, 2nd operand of multiplication
Pr : Product, result of multiplication
Rem : Remainder
Quo : Quotient, result of division
...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

I/O Ports

The SAB 80C517 has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517 has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

Power Saving Modes

The SAB 80C517 provides – due to Siemens ACMOS technology – three modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with the eighth part of its normal operating frequency. Slowing down the frequency greatly reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied by the clock and able to work.
- The **Power Down Mode**
  Operation of the SAB 80C517 is stopped, the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.

All of these modes are entered by software. Special function register PCON (power control register, address is 87H) is used to select one of these modes.

Hardware Enable for Power Saving Modes

A dedicated Pin ($\overline{PE}$/SWD) of the SAB 80C517 allows to block the power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer (see there for further description).

$\overline{PE}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The instruction sequences used for entering of these modes will not affect the normal operation of the device.
$\overline{PE}$/SWD = V_{IL} (logic low level):	All power saving modes can be activated by software. When left unconnected, Pin $\overline{PE}$/SWD is pulled to high level by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin $\overline{PE}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 7.

Table 7
Status of External Pins During Idle and Power Down

Outputs	Last instruction executed from internal code memory		Last instruction executed from external code memory	
	Idle	**Power down**	**Idle**	**Power Down**
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
Port 0	Data	Data	Float	Float
Port 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 2	Data	Data	Address	Data
Port 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 4	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 5	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 6	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output

Idle Mode

During idle mode all peripherals of the SAB 80C517 are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to entering the power down mode.
The two bits IDLE and IDLS must be set by to consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levels (see table 7).

Table 8
Baud Rate Generation

Function		Serial Interface 0		Serial Interface 1
8-Bit synchronous channel	**Mode**	**Mode 0**		–
	Baud rate *)	1 MHz @ f_{OSC} = 12 MHz		–
	Baud rate derived from	f_{OSC}		–
8-Bit UART	**Mode**	**Mode 1**		**Mode B**
	Baud rate *)	1 – 62.5 K	4800, 9600	1.5 – 375 K
	Baud rate derived from	Timer 1	BD	8-bit baud rate generator
9-Bit UART	**Mode**	**Mode 2**	**Mode 3**	**Mode A**
	Baud rate *)	187.5 K/ 375 K	1 – 62.5 K	1.5 – 375 K
	Baud rate derived from	$f_{OSC}/2$	Timer 1	8-bit baud rate generator

*) Baud rate values are given for 12 MHz oscillator frequency.

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through R × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or from the oscillator via a special prescaler ("BD").

Timer 1 may be operated in mode 1 (to generate slow baud rates) or mode 2. The dedicated baud rate generator "BD" provides the two standard baud rates 4800 or 9600 baud. Table 8 shows possible configurations and the according baud rates.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T×D0) or received (through R×D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On trans- mission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T×D1) or received (through R×D1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1

Variable baud rates for modes A and B of serial interface 1 can be derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by a 8-bit free running timer with programmable reload register.

Watchdog Units

The SAB 80C517 offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

- programmable watchdog timer (WDT), variable from 512 µs up to about 1.1 s time out period @12 MHz. Upward compatible to SAB 80515 watchdog.
- oscillator watchdog (OWD), monitors the on-chip oscillator and forces the micro-controller to go into reset state, in case the on-chip oscillator fails.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{\text{PE}}$/SWD (Pin 4) is held high during RESET. The SAB 80C517 then starts program execution with the WDT running. Pin $\overline{\text{PE}}$/SWD doesn't allow dynamic switching of the WDT.

Software initialization is done by setting bit SWDT. A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 11.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be manipulated by software.

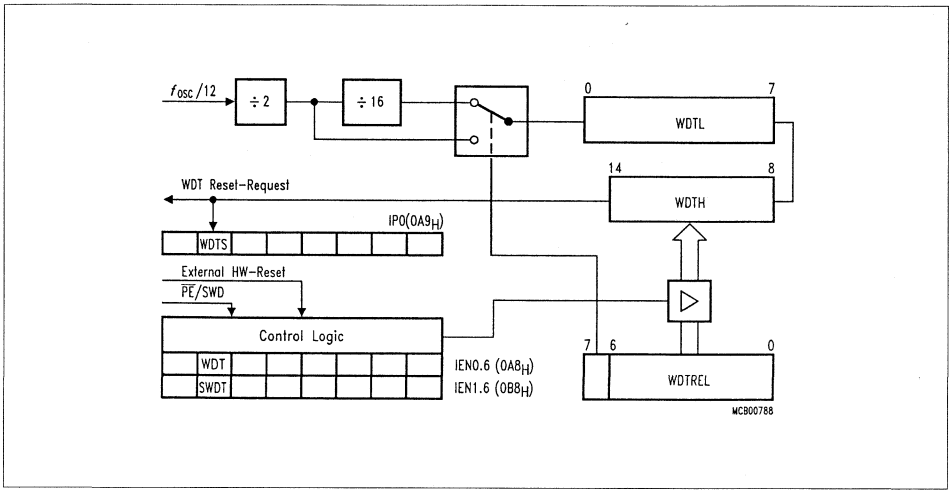


Figure 11
Block Diagram of the Programmable Watchdog Timer

Oscillator Watchdog

The oscillator watchdog monitors the on-chip quartz oscillator. A detected oscillator failure (f_{OSC} < appr. 300 kHz) causes a hardware reset. The reset state is held until the on-chip oscillator is working again. The oscillator watchdog feature is enabled by a high level at pin OWE (pin 69). An oscillator watchdog reset sets status flag OWDS which can be examined and modified by software. Figure 12 shows a block diagram of the oscillator watchdog.

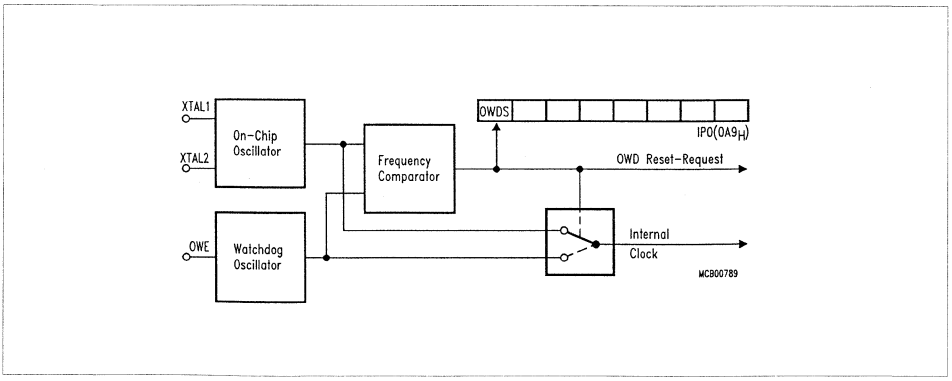


Figure 12
Functional Block Diagram of the Oscillator Watchdog

Instruction Set Summary

The SAB 80C517/80C537 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80C517/83C537 ..... 0 to 70 °C
SAB 80C517/83C537-T40/85 ..... – 40 to 85 °C
Storage temperature T_{ST} ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10mA to +10mA
Absolute sum of all input currents during overload condition ..... |100mA|
Power dissipation ..... 2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

$V_{CC} = 5$ V ± 10 %; $V_{SS} = 0$ V;
$T_A = 0$ to 70 °C for the SAB 80C517/83C537
$T_A = -40$ to 85 °C for the SAB 80C517-/83C537-T40/85

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$)	V_{IL}	– 0.5	0.2 V_{CC} – – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – – 0.3	V	–
Input high voltage	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3, 4, 5, 6)	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1)]

Notes see page 265.

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OL1}	–	0.45	V	I_{OL}=3.2mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH}=–80 µA I_{OH}=–10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH}=–800 µA[2] I_{OH}=–80 µA[2]
Logic 0 input current (ports 1, 2, 3, 4, 5, 6)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current (OWE, $\overline{PE}$/SWD)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, ports 7, 8)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC} [10]
Pin capacitance	C_{IO}	–	10	pF	f_C= 1 MHz T_A= 25 °C
Power supply current: Active mode, 12 MHz [6] Idle mode, 12 MHz [6] Slow down mode, 12 MHz [6] Active mode, 16 MHz [6] Idle mode, 16 MHz [6] Slow down mode, 16MHz [6] Power down Mode	 I_{CC} I_{CC} I_{PD}	 – – – – – – –	 40 15 15 52.3 19 19 50	 mA mA mA mA mA mA µA	 V_{CC} = 5 V,[4] V_{CC} = 5 V,[5] V_{CC} = 5 V,[5] V_{CC} = 5 V,[4] V_{CC} = 5 V,[5] V_{CC} = 5 V,[5] V_{CC} = 2...5.5 V [3]

Notes see page 265.

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V; $V_{IntAREF}$ - $V_{IntAGND}$ ≥ 1V
T_A = 0 to 70 °C for the SAB 80C517/83C537
T_A = – 40 to 85 °C for the SAB 80C517/83C537-T40/875

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
Analog input capacitance	C_I	–	25	60	pF	7)
Load time	t_L	–	–	2 t_{CY}	µs	7)
Sample time (incl. load time)	t_S	–	–	7t_{CY}	µs	7)
Conversion time (incl. sample time)	t_C	–	–	13 t_{CY}	µs	7)
Differential non-linearity Integral non-linearity Offset error Gain error Total unadjusted error	DNLE INLE TUE	– – 	± 1/2 ± 1/2 ± 1/2 ± 1/2 ± 1	± 1 ± 1 ± 1 ± 1 ± 2	LSB LSB LSB LSB LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 7)
Internal reference error	$V_{IntREFERR}$	–		± 30	mV	8)
V_{AREF} supply current	I_{REF}	–	–	5	mA	8)

Notes see page 265.

Notes for pages 262, 263 and 264:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt- trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Power down I_{PD} is measured with all output pins disconnected;
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
V_{AGND}= N.C.; V_{AREF} = V_{CC}; $\overline{PE}$/SWD = OWE = V_{SS}.

4) I_{CC} (active mode) is measured with all output pins disconnected; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
$\overline{EA}$ = OWE = $\overline{PE}$/SWD = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC};
$\overline{RESET}$ = V_{SS}. I_{CC} would be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode,) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
$\overline{RESET}$ = OWE = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}.
I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL = N.C.; Port 7 = Port 8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}.

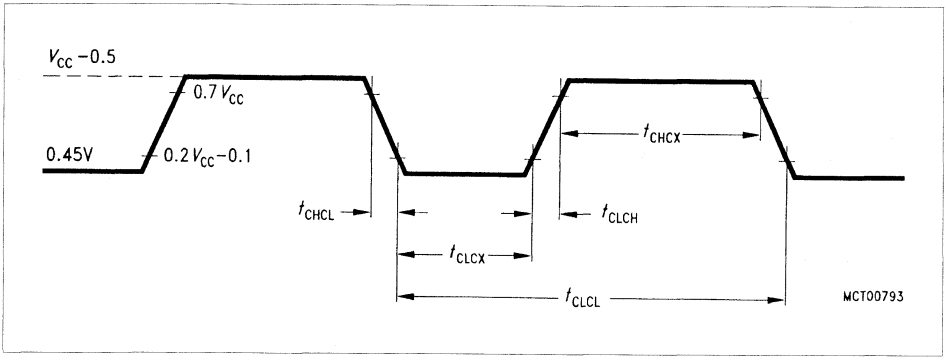
6) I_{CC} (max.) at other frequencies is given by: active mode: I_{CC} max = 3.1 * f_{OSC} + 3.0
idle mode: I_{CC} max = 1.0 * f_{OSC} + 3.0
Where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5).

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (T_L). After charging of the internal capacitance (C_I) in the load time (T_L) the analog input must be held constant for the rest of the sample time (T_S).

8) The differential impedance R_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding the limit values at one or more input channels will cause additional current which is sinked sourced at these channels. This may also affect the accuracy of other channels which are operated within the specification.

10) Only valid for not selected analog inputs.



Clock of Waveform for I_{CC} Tests in Active, Idle Mode and Slow Down Mode

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB 80C517/83C537
T_A = – 40 to 85 °C for the SAB 80C517/83C537-T40/85
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF))

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	53	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	48	–	$t_{CLCL} - 35$	–	ns
Address to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$ *)	t_{PXIX}*)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$ *)	t_{PXAV}*)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instruction in	t_{AVIV}	–	302	0	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	–	–	–		ns

*) Interfacing the SAB 80C517 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid instr in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWX}	433	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C517-16/83C537-16

T_A = – 40 to 85 °C for the SAB 80C517-16/83C537-16-T40/85

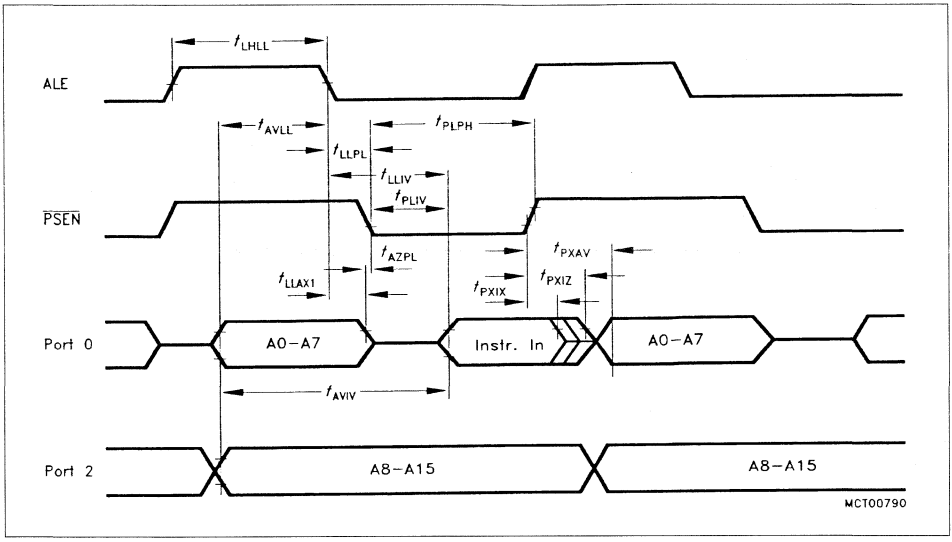
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	33	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	28	–	$t_{CLCL} - 35$	–	ns
Address to valid instr. in	t_{LLIV}	–	150	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr. in	t_{PLIV}	–	88	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float *) after $\overline{PSEN}$	t_{PXIZ}	–	43	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$ *)	t_{PXAV}	55	–	$t_{CLCL} - 8$	–	ns
Address to valid instr. in	t_{AVIV}	–	198	0–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

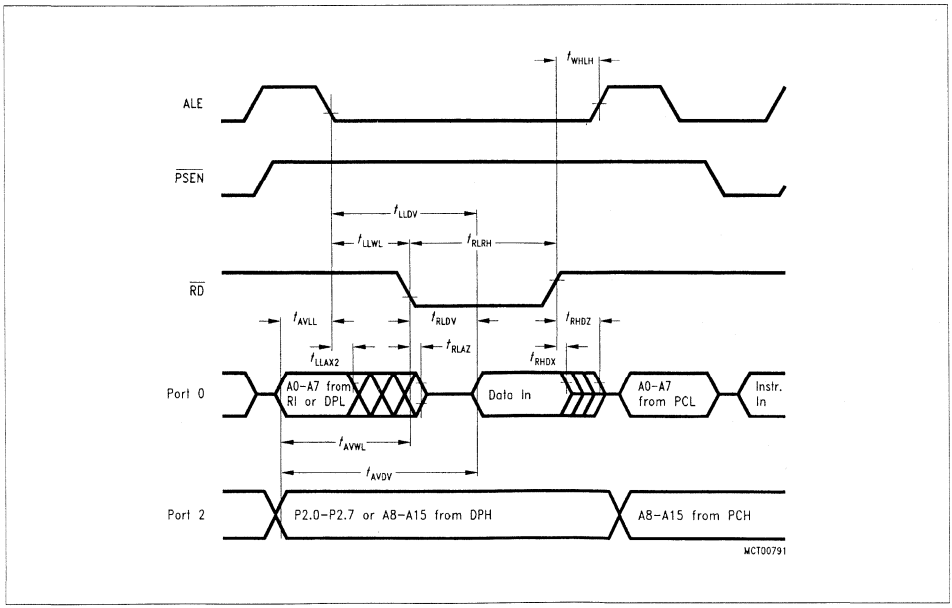
*) Interfacing the SAB 80C517 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

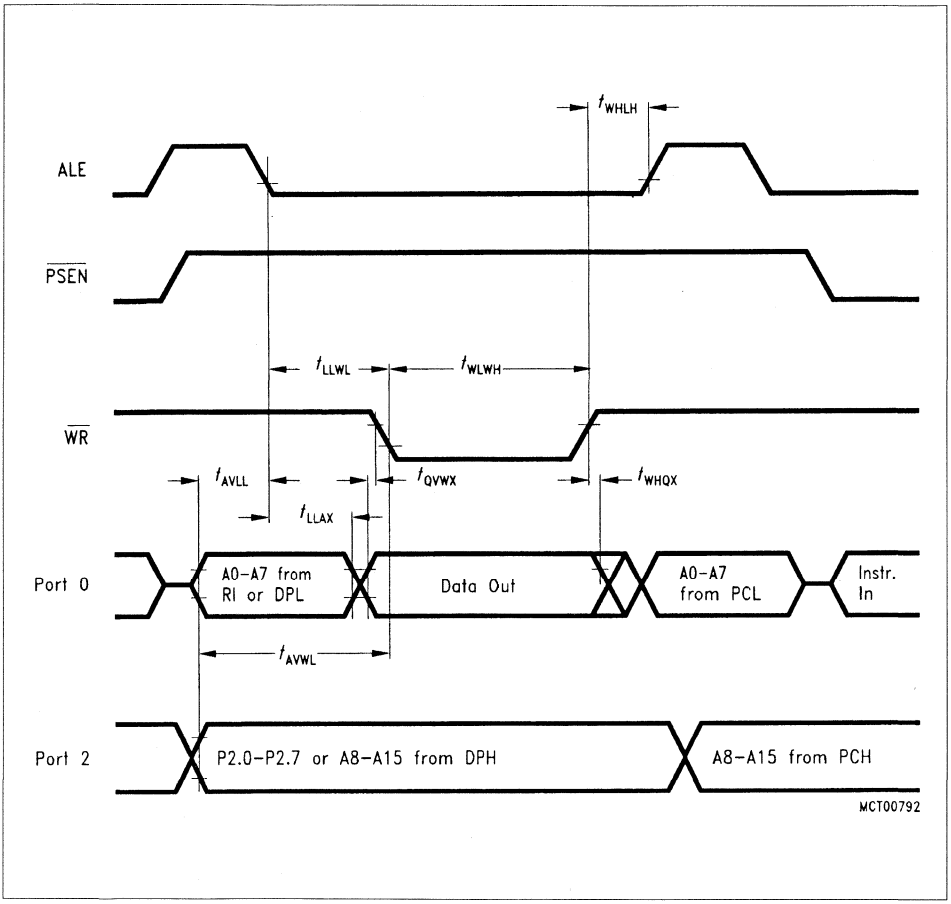
Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



Data Memory Read Cycle



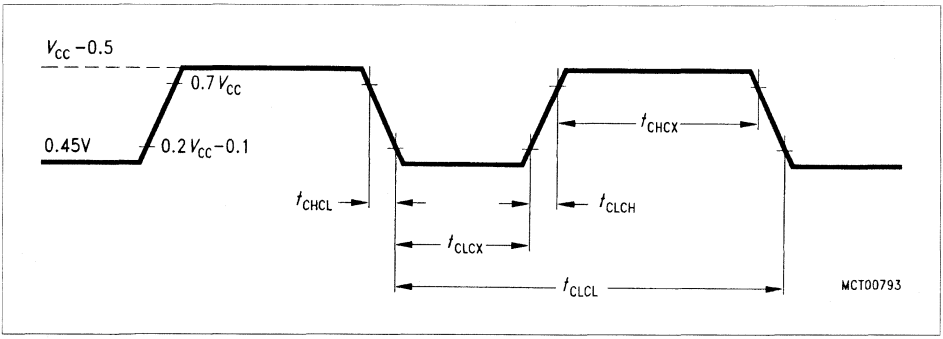
Data Memory Write Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 12 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	83.3	285	ns
Oscillator frequency	$1/t_{CLCL}$	3.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1 MHz to 16 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	62.5	285	ns
Oscillator frequency	$1/t_{CLCL}$	3.5	16	MHz
High time	t_{CHCX}	25	–	ns
Low time	t_{CLCX}	25	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



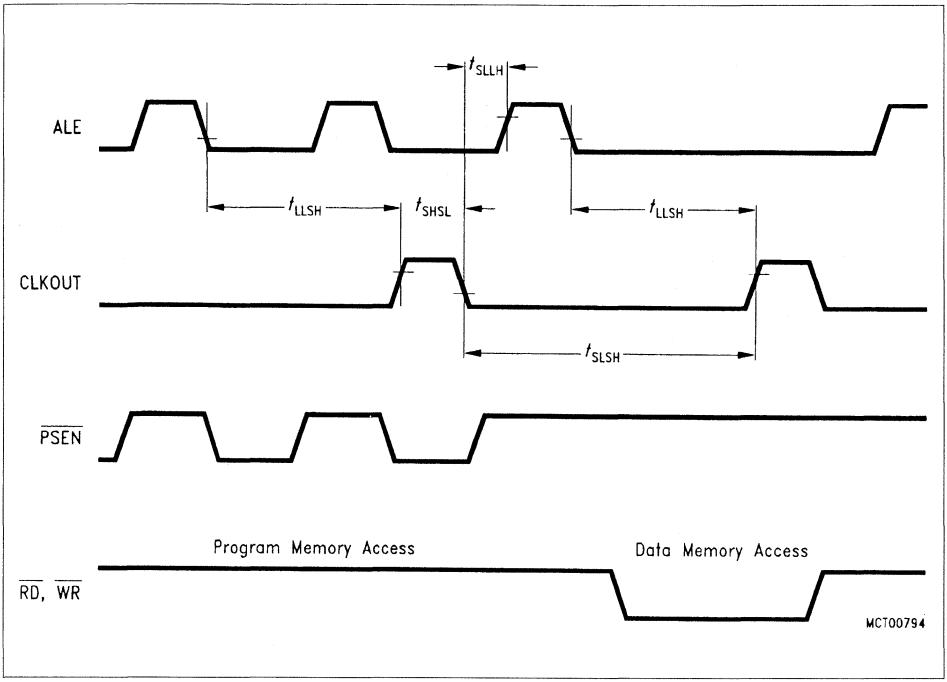
External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	398	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	85	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	585	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

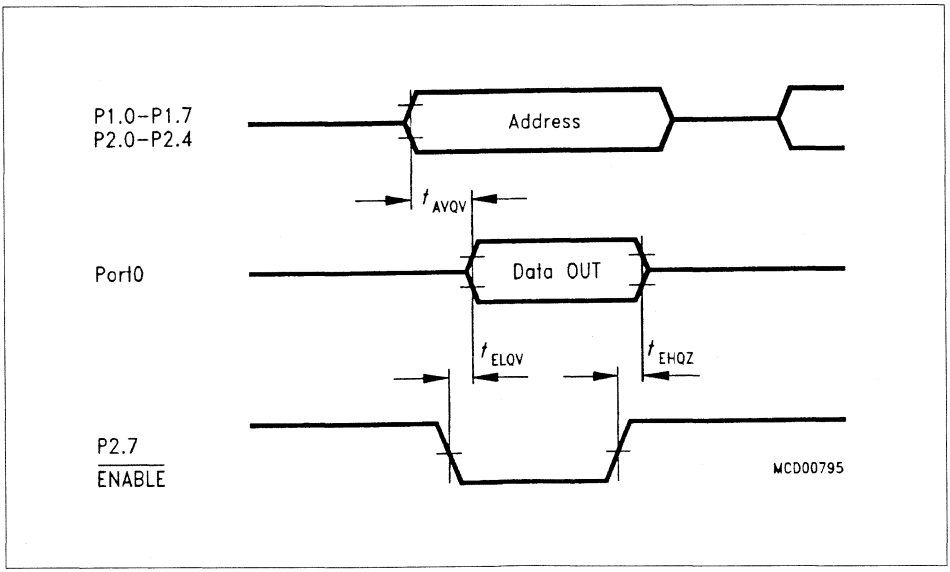


System Clock Timing

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

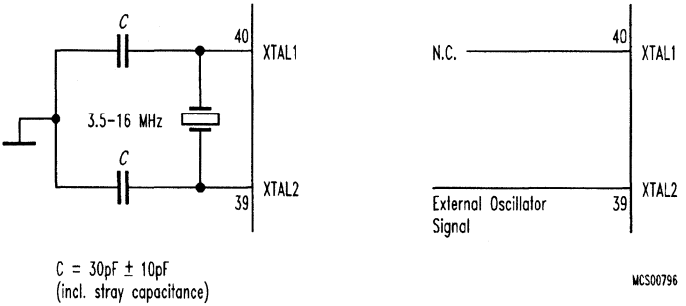
Parameter	Symbol	Limit values		Unit
		min	max.	
ROM Verification				
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



ROM Verification

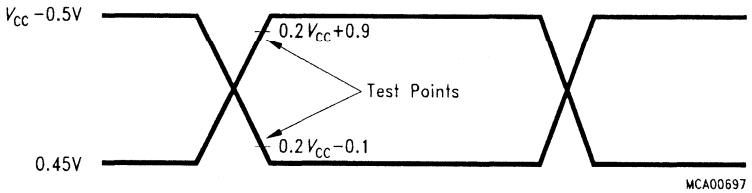
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA

Recommended Oscillator Circuits



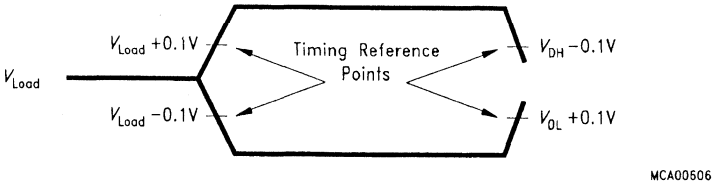
C 30 pF ± 10 pF
(incl. stray capacitance)

AC Testing



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic 1 and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Input, Output Waveforms



Float Waveforms

SMD = Surface Mounted Device

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

SAB 80C517A/83C517A-5

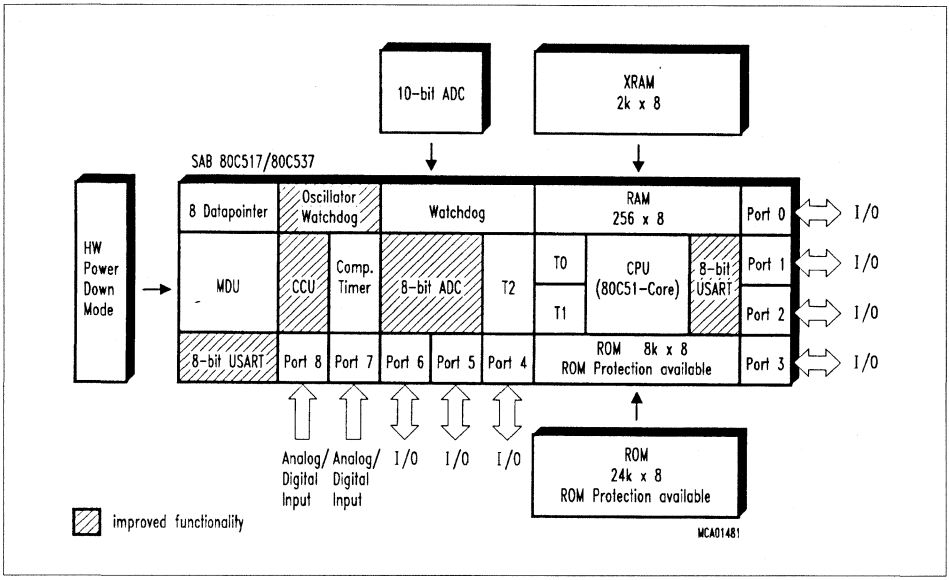
Preliminary

SAB 83C517A-5	Microcontroller with factory mask-programmable ROM
SAB 80C517A	Microcontroller for external ROM

- SAB 80C517A/83C517A-5, up to 18 MHz operation
- 32 K × 8 ROM (SAB 83C517A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- 2 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 666 ns instruction cycle time at 18 MHz
  - 256 directly addressable bits
  - Boolean processor
  - 64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Seventeen interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 12 multiplexed inputs
- Two full duplex serial interfaces with programmable Baudrate-Generators
- Fully upward compatible with SAB 80C515, SAB 80C517, SAB 80C515A
- Extended power saving mode
- Fast Power-On Reset
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85°C (T3)
  – 40 to 110°C (T4)
- Plastic packages: P-LCC-84, P-MQFP-100-2

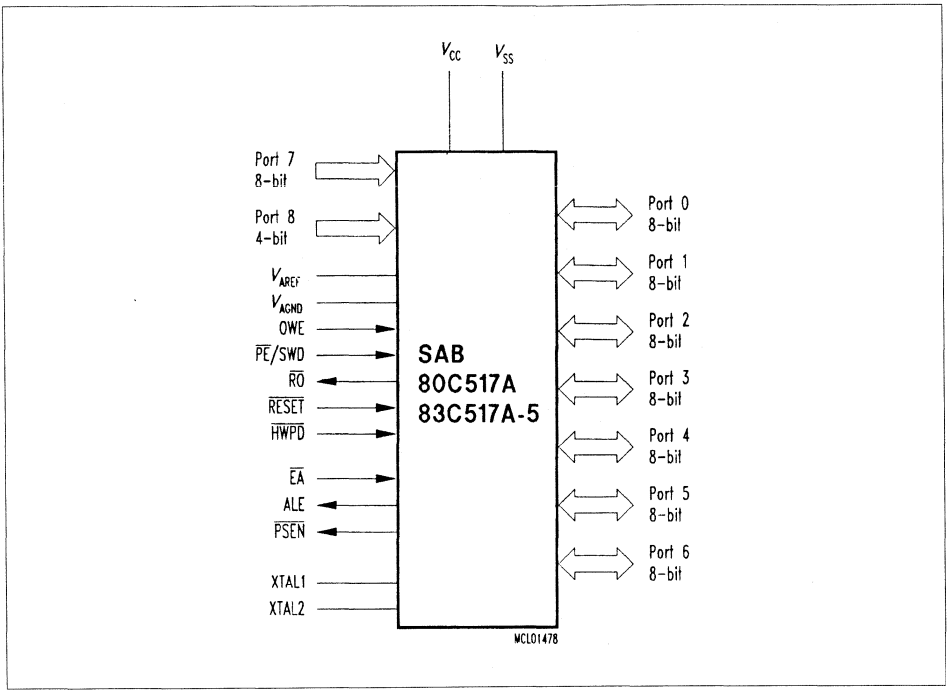
The SAB 80C517A/83C517A-5 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C517 features and operating characteristics the SAB 80C517A is expanded in its "fail-safe" characteristics and timer capabilities.The SAB 80C517A is identical with the SAB 83C517A-5 except that it lacks the on-chip program memory. The SAB 80C517A/83C517A-5 is supplied in a 84-pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad flat package (P-MQFP-100-2).



Ordering Information

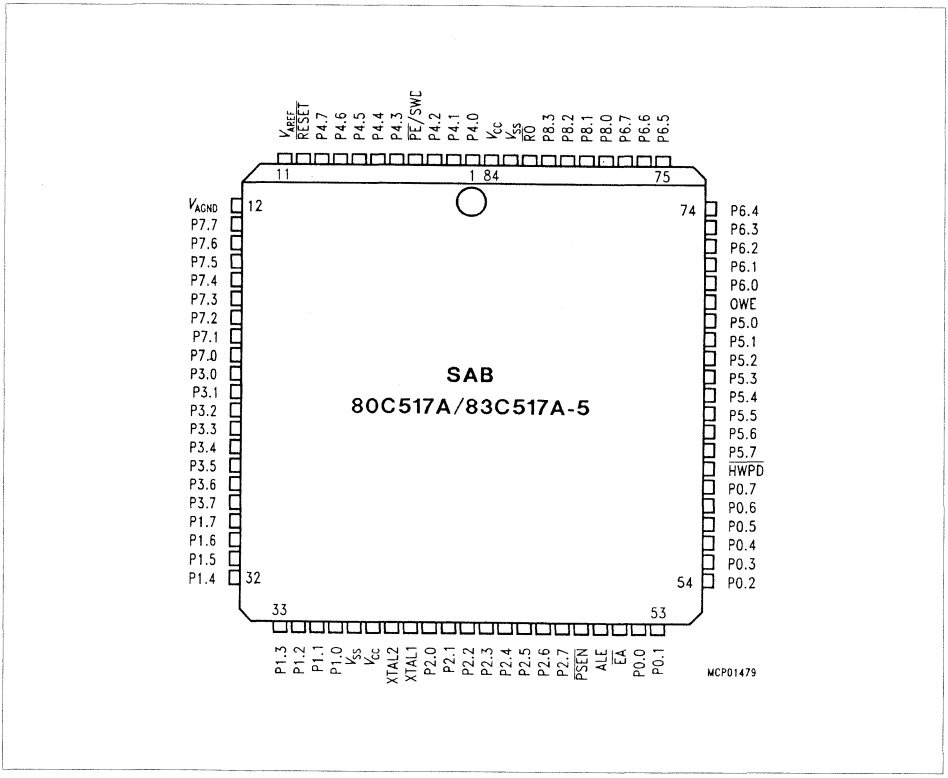
Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C517A-N18	Q67120-C583	P-LCC-84	for external memory,18 MHz
SAB 80C517A-M18	TBD	P-MRFP-100	
SAB 83C517A-5N18	Q67120-C582	P-LCC-84	with mask-programmable ROM, 18 MHz
SAB 80C517A-N18-T3	Q67120-C769	P-LCC-84	for external memory,18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-5N18-T3	Q67120-C771	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-N18-T4	TBD	P-LCC-84	for external memory, 18 MHz ext. temperature -40 to +110°C
SAB 83C517A-5N18-T4	TBD	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature -40 to +110°C



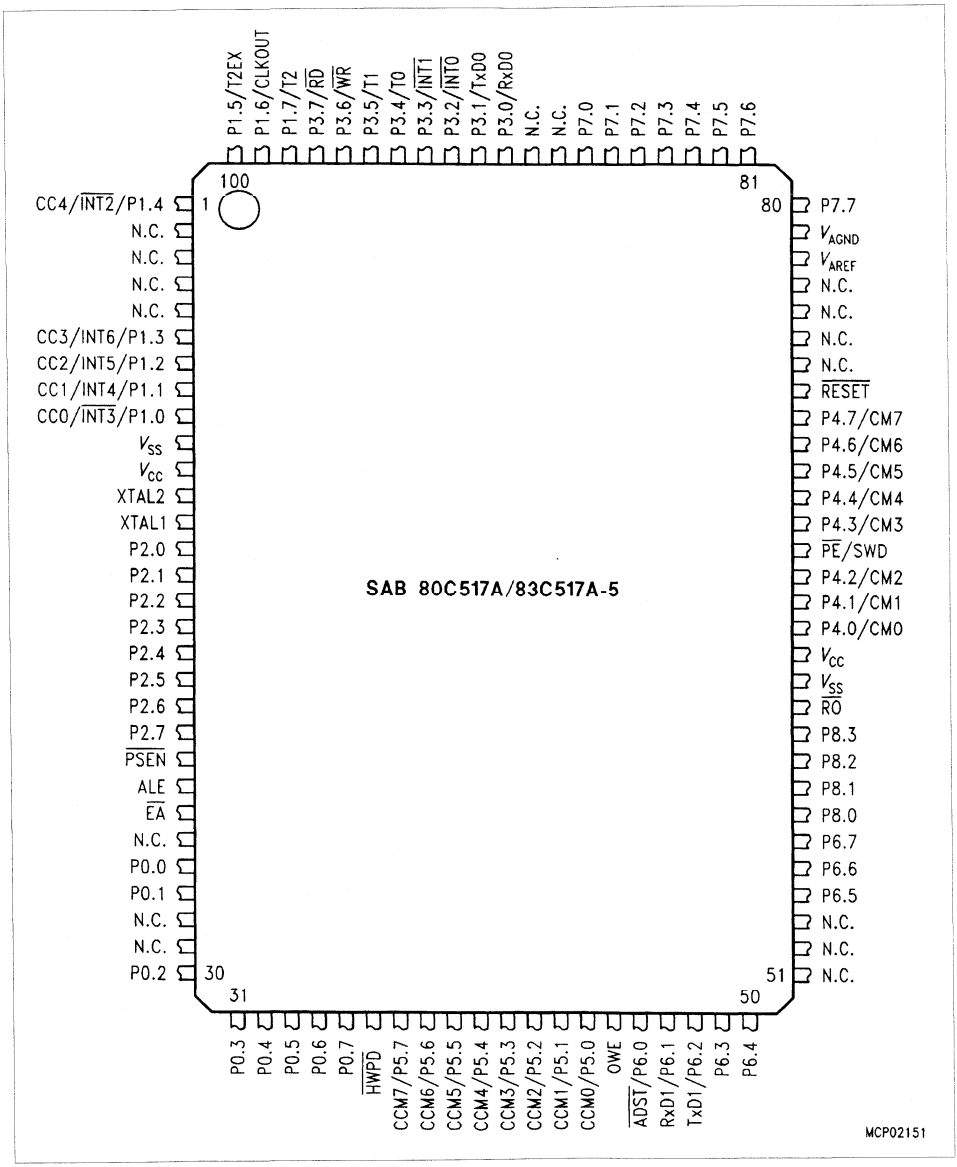
Logic Symbol

The pin functions of the SAB 80C517A are identical with those of the SAB 80C517/80C537 with one exception:

Typ	SAB 80C517A	SAB 80C517/80C537
P-LCC-84, Pin 60	$\overline{\text{HWPD}}$	N.C.
P-MQFP-100-2,Pin 36		



Pin Configuration
(P-LCC-84)



Pin Configuration
(P-MQFP-100-2)

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P4.0 – P4.7	1– 3, 5 – 9	64 - 66, 68 - 72	I/O	**Port 4** is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
$\overline{PE}$/SWD	4	67	I	**Power saving modes $\overline{enable}$ Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{RESET}}$	10	73	I	$\overline{\text{RESET}}$ A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	78		**Reference voltage** for the A/D converter.
V_{AGND}	12	79		**Reference ground** for the A/D converter.
P7.7 -P7.0	13 - 20	80 - 87	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P3.0 - P3.7	21 - 28	90 - 97	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D0 (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D0 (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control – $\overline{INT0}$ (P3.3): interrupt 1 input/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P1.7 - P2.0	29 - 36	98 - 100, 1, 6 - 9	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. It is used for the low order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): $\overline{\text{interrupt 3 input}}$/ compare 0 output /capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output /capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output /capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output /capture 3 input – $\overline{\text{INT2}}$/CC4 (P1.4): $\overline{\text{interrupt 2 input}}$ / compare 4 output /capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
XTAL2	39	12	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	13	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is devided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	41 - 48	14 - 21	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{PSEN}$	49	22	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	23	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access
$\overline{EA}$	51	24	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB 83C517A-5 only) when the PC is less than 8000H. When held at low level, the SAB 80C517A fetches all instructions from external program memory. For the SAB 80C517A this pin must be tied low
P0.0 - P0.7	52 - 59	26 - 27, 30 - 35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impe-dance inputs. Port 0 is also the multiplexed low-order a8ddress and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also out-puts the code bytes during program verifica-tion in the SAB 83C517A if ROM-Protection was not enabled. External pull-up resistors are required during program verification.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{HWPD}}$	60	36	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (see table 7)
P5.7 - P5.0	61 - 68	37 - 44	I/O I	**Port 5** is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare" and "Set/Reset Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 to CCM7 (P5.0 to P5.7): concurrent compare or Set/Reset
OWE	69	45	I/O	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P6.0 - P6.7	70 - 77	46 - 50, 54 - 56	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: $\overline{ADST}$ (P6.0): external A/D converter start pin – $R_x D1$ (P6.1): receiver data input of serial interface 1 – $T_x D1$ (P6.2): transmitter data output of serial interface 1
P8.0 - P8.3	78 - 81	57 - 60	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{RO}$	82	61	O	**Reset Output** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low.
V_{SS}	37, 83	10, 62	–	**Circuit ground potential**
V_{CC}	38, 84	11, 63	–	**Supply Terminal** for all operating modes
N.C.	–	2 - 5, 25, 28 - 29, 51 - 53, 74 - 77, 88 - 89	–	Not connected

* I = Input
O = Output

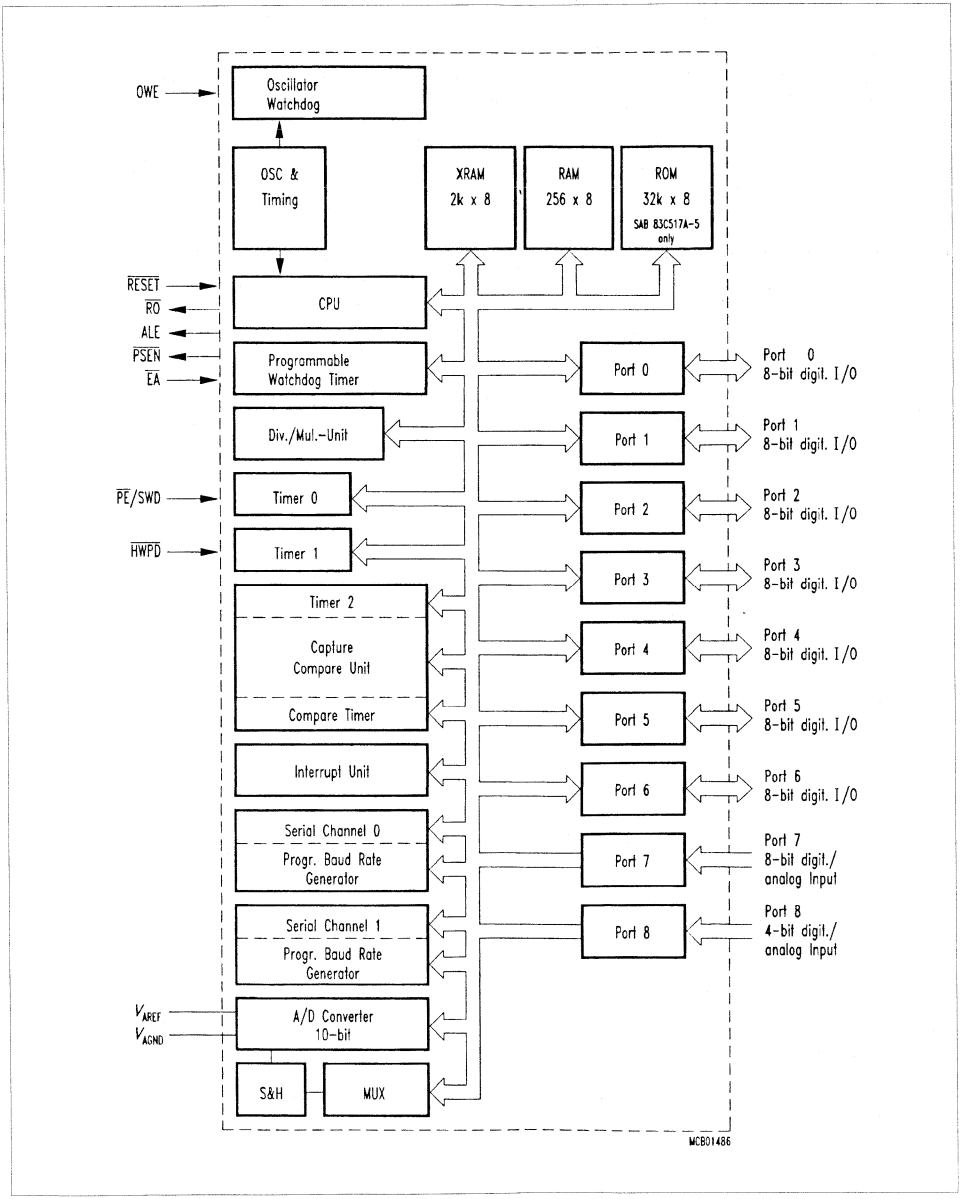


Figure 1
Block Diagram

Functional Description

The SAB 80C517A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C517. The SAB 80C517A is therefore compatible with code written for the SAB 80C517.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517A's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

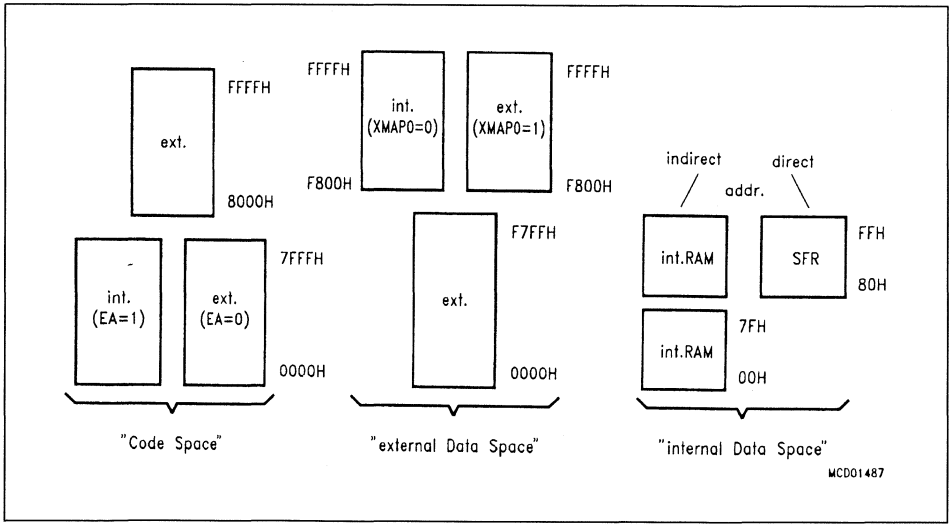


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C517A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C517A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ controls whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C517A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask.Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	ROM-Verification Mode (see 'AC Characteristics')	Restrictions
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Code Space')

The data memory space consists of an internal and an external memory space. The SAB 80C517A contains another 2 Kbyte on On-Chip RAM above the 256-bytes internal RAM of the base type SAB 80C517. This RAM is called XRAM in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers. Registers XPAGE and SYSCON are controlling whether data fetches at addresses F800H to FFFFH are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

- the lower 128 bytes of RAM including four banks containing eight registers each
- the upper 128 byte of RAM
- the 128 byte special function register area.
- a 2 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from F800H to FFFFH. Special Function Register SYSCON controls whether data is read or written to XRAM or external RAM.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes (see User's Manual SAB 80C517). The stack can be located anywhere in the internal data memory.

Architecture for the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range (F800H-FFFFH). It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C517A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geqq$ F800H).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C517A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91H									XPAGE

The reset value of XPAGE is 00H.
XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C517A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM: The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.

b) Access to external memory: The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C517A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. 0B1H	—	—	—	—	—	—	XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 = 0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for $\overline{RD}$/$\overline{WR}$ signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is xxxx xx01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C517A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the externa $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

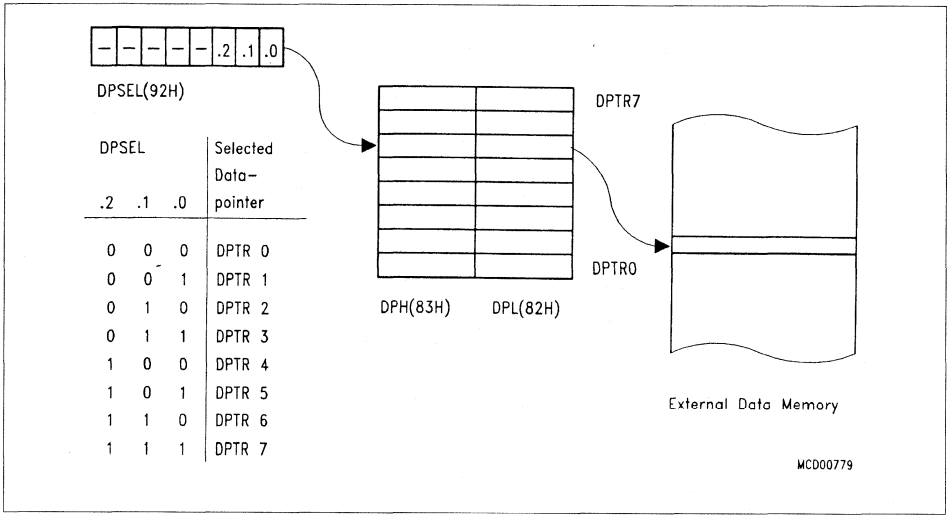
Table 1:
Behaviour of P0/P2 and RD/WR during MOVX accesses

		EA = 0			EA = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used
	DPTR ≥ XRAM address range	a) P0/P2→BUS (WR -Data only) b) RD/WR inactive c) XRAM is used	a) P0/P2→BUS (WR -Data only) b) RD/WR active c) XRAM is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used	a) P0/P2→I/0 b) RD/WR inactive c) XRAM is used	a) P0/P2→BUS (WR -Data only) b) RD/WR active c) XRAM is used	a) P0/P2→Bus b) RD/WR active c) ext. memory is used
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used
	XPAGE ≥ XRAM addr. page range	a) P0/P2→BUS (WR -Data only) P2→I/0 b) RD/WR inactive c) XRAM is used	a) P0/P2→BUS (WR -Data only) P2→I/0 b) RD/WR active c) XRAM is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used	a) P0/P2→I/0 b) RD/WR inactive c) XRAM is used	a) P0→BUS (WR -Data only) P2→I/0 b) RD/WR active c) XRAM is used	a) P0→Bus P2→I/0 b) RD/WR active c) ext. memory is used

modes compatible to 8051 - family

Multiple Datapointers

As a functional enhancement to standard 8051 controllers, the SAB 80C517A contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in special function register DPSEL (data pointer select, addr. 92H). Figure 3 illustrates the addressing mechanism.



DPSEL .2	.1	.0	Selected Data-pointer
0	0	0	DPTR 0
0	0	1	DPTR 1
0	1	0	DPTR 2
0	1	1	DPTR 3
1	0	0	DPTR 4
1	0	1	DPTR 5
1	1	0	DPTR 6
1	1	1	DPTR 7

Figure 3
Addressing of External Data Memory

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 1 and table 2.

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80C517A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**S0CON** [1]	**00H**
81H	SP	07H	99H	S0BUF	XXH
82H	DPL	00H	9AH	IEN2	XX00 00X0B
83H	DPH	00H	9BH	S1CON	0X00 0000B
84H	(WDTL) [3]	(00H)	9CH	S1BUF	XXH
85H	(WDTH) [3]	(00H)	9DH	S1RELL	00H
86H	WDTREL	00H	9EH	reserved	XXH
87H	PCON	00H	9FH	reserved	XXH
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	COMSETL	00H
8AH	TL0	00H	A2H	COMSETH	00H
8BH	TL1	00H	A3H	COMCLRL	00H
8CH	TH0	00H	A4H	COMCLRH	00H
8DH	TH1	00H	A5H	SETMSK	00H
8EH	reserved	XXH [2]	A6H	CLRMSK	00H
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	XPAGE	00H	A9H	IP0	00H
92H	DPSEL	XXXXX000B	AAH	SRELL	0D9H [3]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3** [1]	**0FFH**	**D0H**	**PSW** [1]	**00H**
B1H	SYSCON	XXXX XX01B	D1H	IRCON1	00H
B2H	reserved	XXH [2]	D2H	CML0	00H
B3H	reserved	XXH [2]	D3H	CMH0	00H
B4H	reserved	XXH [2]	D4H	CML1	00H
B5H	reserved	XXH [2]	D5H	CMH1	00H
B6H	reserved	XXH [2]	D6H	CML2	00H
B7H	reserved	XXH [2]	D7H	CMH2	00H
B8H	**IEN1** [1]	**OOH**	**D8H**	**ADCON0** [1]	00H
B9H	IP1	XX00 0000B	D9H	ADDATH	00H
BAH	S0RELH	XXXX XX11B	DAH	ADDATL	00H
BBH	S1RELH	XXXX XX11B	DBH	P7	XXH
BCH	reserved	XXH	DCH	ADCON1	XXXX 0000B
BDH	reserved	XXH	DDH	P8	XXH
BSH	reserved	XXH	DEH	CTRELL	00H
BFH	reserved	XXH	DFH	CTRELH	00H
C0H	**IRCON0** [1]	**00H**	**E0H**	**ACC** [1]	**00H**
C1H	CCEN	00H	E1H	CTCON	0X00 000B
C2H	CCL1	00H	E2H	CML3	00H
C3H	CCH1	00H	E3H	CMH3	00H
C4H	CCL2	00H	E4H	CML4	00H
C5H	CCH2	00H	E5H	CMH4	00H
C6H	CCL3	00H	E6H	CML5	00H
C7H	CCH3	00H	E7H	CMH5	00H
C8H	**T2CON** [1]	**00H**	**E8H**	**P4** [1]	**0FFH**
C9H	CC4EN	00H	E9H	MD0	XXH
CAH	CRCL	00H	EAH	MD1	XXH
CBH	CRCH	00H	EBH	MD2	XXH
CCH	TL2	00H	ECH	MD3	XXH
CDH	TH2	00H	EDH	MD4	XXH
CEH	CCL4	00H	EEH	MD5	XXH
CFH	CCH4	00H	EFH	ARCON	0XXX XXXXB

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B** [1]	**00H**	**F8H**	**P5** [1]	**0FFH**
F1H	reserved	XXH	F9H	reserved	XXH
F2H	CML6	00H	FAH	P6	0FFH
F3H	CMH6	00H	FBH	reserved	XXH
F4H	CML7	00H	FCH	reserved	XXH
F5H	CMH7	00H	FDH	(IS0)	XXH
F6H	CMEN	00H	FEH	(IS1)	XXH
F7H	CMSEL	00H	FFH	reserved	XXH

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H** [1]	00H
	B	B-Register	**0F0H** [1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	DPSEL	Data Pointer Select Register	92h	XXXX X000B[3]
	PSW	Program Status Word Register	**0D0H** [1]	00H
	SP	Stack Pointer	81H	07H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**0D8H** [1]	00H
	ADCON1	A/D Converter Control Register 1	0DCH	00H
	ADDATH	A/D Converter Data Reg. High Byte	0D9H	00H
	ADDATL	A/D Converter Data Reg. Low Byte	0DAH	00H
Interrupt System	IEN0	Interrupt Enable Register 0	**0A8H** [1]	00H
	CTCON [2]	Com. Timer Control Register	0E1H	0X00 0000B
	IEN1	Interrupt Enable Register 1	**0B8H** [1]	00H
	IEN2	Interrupt Enable Register 2	9AH	XX00 00X0B [3]
	IP0	Interrupt Priority Register 0	0A9H	00H
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000B
	IRCON0	Interrupt Request Control Register	**0C0H** [1]	00H
	IRCON1	Interrupt Request Control Register	0D1H	00H
	TCON [2]	Timer Control Register	**88H** [1]	00H
	TCON [2]	Timer 2 Control Register	**0C8H**	00H
MUL/DIV Unit	ARCON	Arithmetic Control Register	0EFH	0XXXX XXXXB
	MD0	Multiplication/Division Register 0	0E9H	XXH
	MD1	Multiplication/Division Register 1	0EAH	XXH
	MD2	Multiplication/Division Register 2	0EBH	XXH
	MD3	Multiplication/Division Register 3	0ECH	XXH
	MD4	Multiplication/Division Register 4	0EDH	XXH
	MD5	Multiplication/Division Register 5	0EEH	XXH

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU) Timer 2	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CC4EN	Comp./Capture Enable 4 Reg.	0C9H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCH4	Comp./Capture Reg. 4, High Byte	0CFH	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CCL4	Comp./Capture Reg. 4, Low Byte	0CEH	00H
	CMEN	Compare Enable Register	0F6H	00H
	CMH0	Compare Register 0, High Byte	0D3H	00H
	CMH1	Compare Register 1, High Byte	0D5H	00H
	CMH2	Compare Register 2, High Byte	0D7H	00H
	CMH3	Compare Register 3, High Byte	0E3H	00H
	CMH4	Compare Register 4, High Byte	0E5H	00H
	CMH5	Compare Register 5, High Byte	0E7H	00H
	CMH6	Compare Register 6, High Byte	0F3H	00H
	CMH7	Compare Register 7, High Byte	0F5H	00H
	CML0	Compare Register 0, Low Byte	0D2H	00H
	CML1	Compare Register 1, Low Byte	0D4H	00H
	CML2	Compare Register 2, Low Byte	0D6H	00H
	CML3	Compare Register 3, Low Byte	0E2H	00H
	CML4	Compare Register 4, Low Byte	0E4H	00H
	CML5	Compare Register 5, Low Byte	0E6H	00H
	CML6	Compare Register 6, Low Byte	0F2H	00H
	CML7	Compare Register 7, Low Byte	0F4H	00H
	CMSEL	Compare Input Select	0F7H	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	COMSETL	Compare Register, Low Byte	0A1	00H
	COMSETH	Compare Register, High Byte	0A2	00H
	COMCLRL	Compare Register, Low Byte	0A3	00H
	COMCLRH	Compare Register, High Byte	0A4	00H
	SETMSK	Mask Register, concerning COMSET	0A5	00H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU), (cont'd)	CLRMSK	Mask Register, concerning COMCLR	0A6	00H
	CTCON	Com. Timer Control Reg.	0E1H	0X00 0000B [3]
	CTRELH	Com. Timer Rel. Reg., High Byte	0DFH	00H
	CTRELL	Com. Timer Rel. Reg., Low Byte	0DEH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON	Timer 2 Control Register	**0C8H** [1]	00H
Ports	P0	Port 0	**80H** [1]	0FFH
	P1	Port 1	**90H** [1]	0FFH
	P2	Port 2	**0A0H** [1]	0FFH
	P3	Port 3	**0B0H** [1]	0FFH
	P4	Port 4	**0E8H** [1]	0FFH
	P5	Port 5	**0F8H** [1]	0FFH
	P6	Port 6,	0FAH	0FFH
	P7	Port 7, Analog/Digital Input	0DBH	
	P8	Port 8, Analog/Digital Input, 4-bit	0DDH	
Pow.Sav. Modes	PCON	Power Control Register	87H	00H
Serial Channels	ADCON0 [2]	A/D Converter Control Reg.	**0D8H** [1]	00H
	PCON [2]	Power Control Register	87H	00H
	S0BUF	Serial Channel 0 Buffer Reg.	99H	0XXH [3]
	S0CON	Serial Channel 0 Control Reg.	**98H** [1]	00H
	S0RELL	Serial Channel 0 Reload Reg., low byte	B2H	D9H
	S0RELH	Serial Channel 0 Reload Reg., high byte	BAH	XXXX.XX11B [3]
	S1BUF	Serial Channel 1 Buffer Reg.,	9CH	0XXH [3]
	S1CON	Serial Channel 1 Control Reg.	9BH	0X00 000B [3]
	S1RELL	Serial Channel 1 Reload Reg., low byte	9DH	00H
	S1RELH	Serial Channel 1 Relaod Reg., high byte	BBH	XXXX.XX11B [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Timer 0/ Timer 1	TCON	Timer Control Register	**88H** [1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**0A8H** [1]	00H
	IEN1 [2]	Interrupt Enable Register 1	**0B8H** [1]	00H
	IP0 [2]	Interrupt Priority Register 0	0A9H	00H
	IP1 [2]	Interrupt Priority Register 1	0B9H	XX00 0000B [3]
	WDTREL	Watchdog Timer Reload Reg.	86H	00H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C517A a new high performance / high-speed 12-channel 10-bit A/D-Converter is implemented. Its successive approximation technique provides 7 µs con-version time (f_{OSC}= 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C517. The main functional blocks are shown in figure 4.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine 10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler (see also Bit ADCL in SFR ADCON 1).

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.33
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	4.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

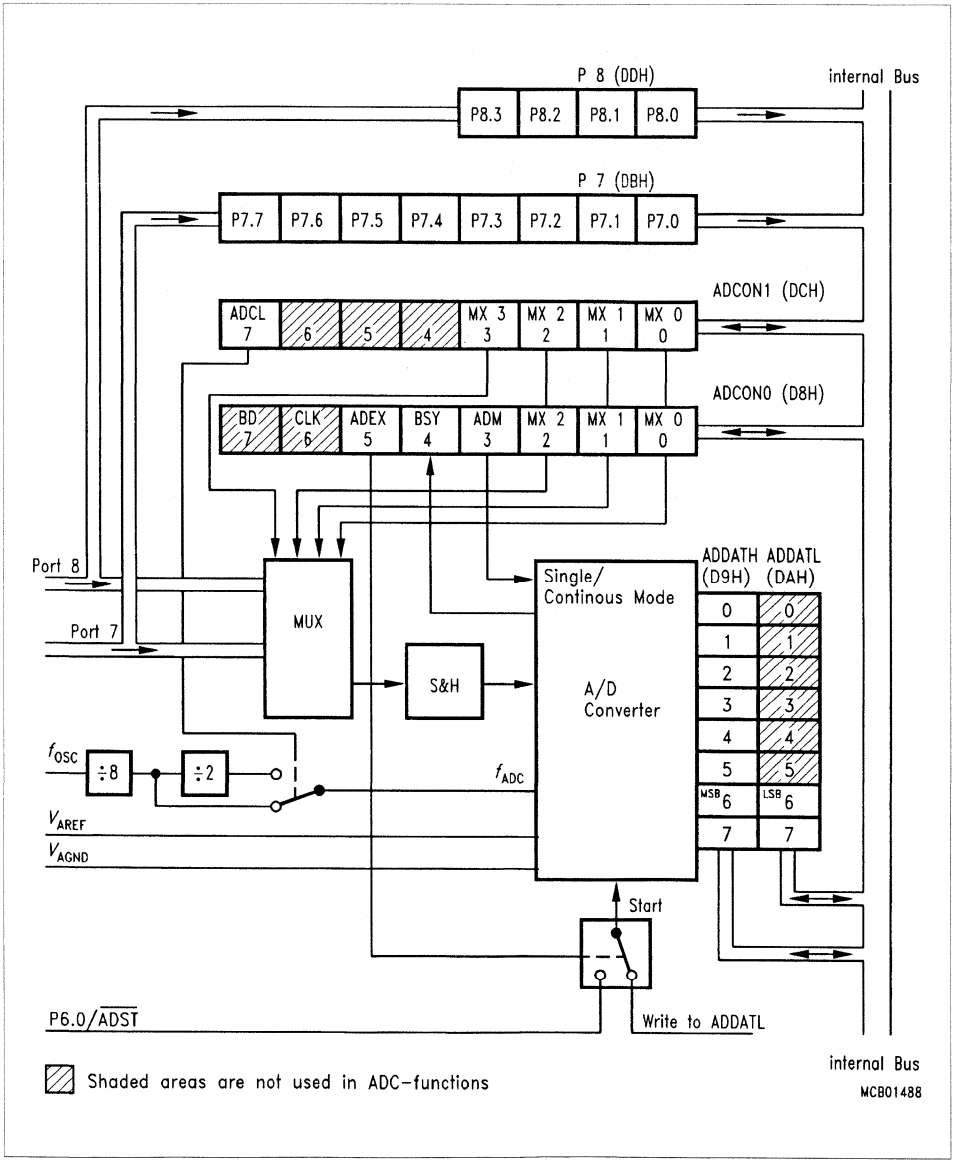


Figure 4
Block Diagram A/D Converter

Compare/Capture Unit (CCU)

The compare/capture unit is a complex timer/register array for applications that require high speed I/O pulse width modulation and more timer/counter capabilities.
The CCU contains

- one 16-bit timer/counter **(timer2)** with 2-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/12}$ (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/2}$ (6 MHz with a 12 MHz crystal).
- fifteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- nine interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers, the compare/reload/capture register and the comset/comclr register are always connected to timer 2. Depending on the register type and the assigned timer three different compare modes can be selected.
Table 3 illustrates possible combinations and the corresponding output lines.

Table 4
CCU Compare Configuration

Assigned Timer	Compare Register	Compare Output	Possible Modes
Timer 2	CRCH/CRCL	P1.0/$\overline{\text{INT3}}$/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/$\overline{\text{INT6}}$/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/$\overline{\text{INT2}}$/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	COMSETL/COMSETH	P5.0/CCM0	Comp. mode 2
		:	:
		P5.7/CCM7	Comp. mode 2
	COMCLRL/	P5.0/CCM0	Comp. mode 2
	COMCLRH	:	:
		P5.7/CCM7	Comp. mode 2
		P4.0/CM0	Comp. mode 1
	CM0H/CM0L	:	:
	:	P4.7/CM7	Comp. mode 1
	CM7H/CM7L		
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with shadow latches)
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with shadow latches)

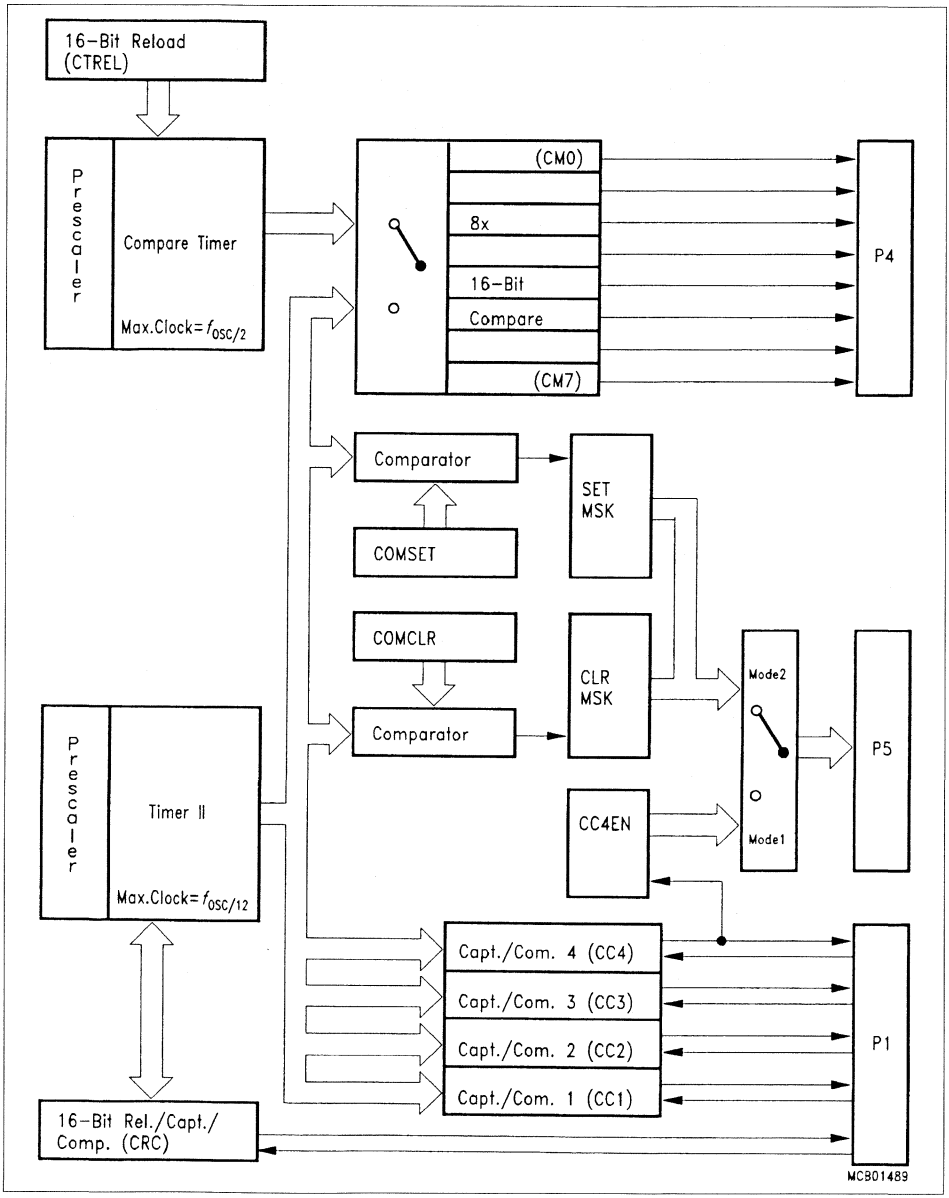


Figure 5
Block Diagram of the Compare/Capture Unit

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored value, an appropriate output signal is generated at the corresponding pin(s) and an interrupt is requested. Three compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It returns to low level at timer overflow.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal does not affect the compare-output.

Mode 2: In compare mode 2 the concurrent compare output pins on Port 5 are used as follows (see figure 9)

- When a compare match occurs with register COMSET, a high level appears at the pins of port 5 whose corresponding bits in the mask register SETMSK (address 0A5H) are set.
- When a compare match occurs in register COMCLR, a low level appears at the pins of port 5 whose corresponding bits in the mask register CLRMSK (address 0A6H) are set.
  Additionally the Port 5 pins used for compare mode 2 may also be directly written to by write instructions to SFR P5. Of course, the pins can also be read under program control.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to 'freeze' the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

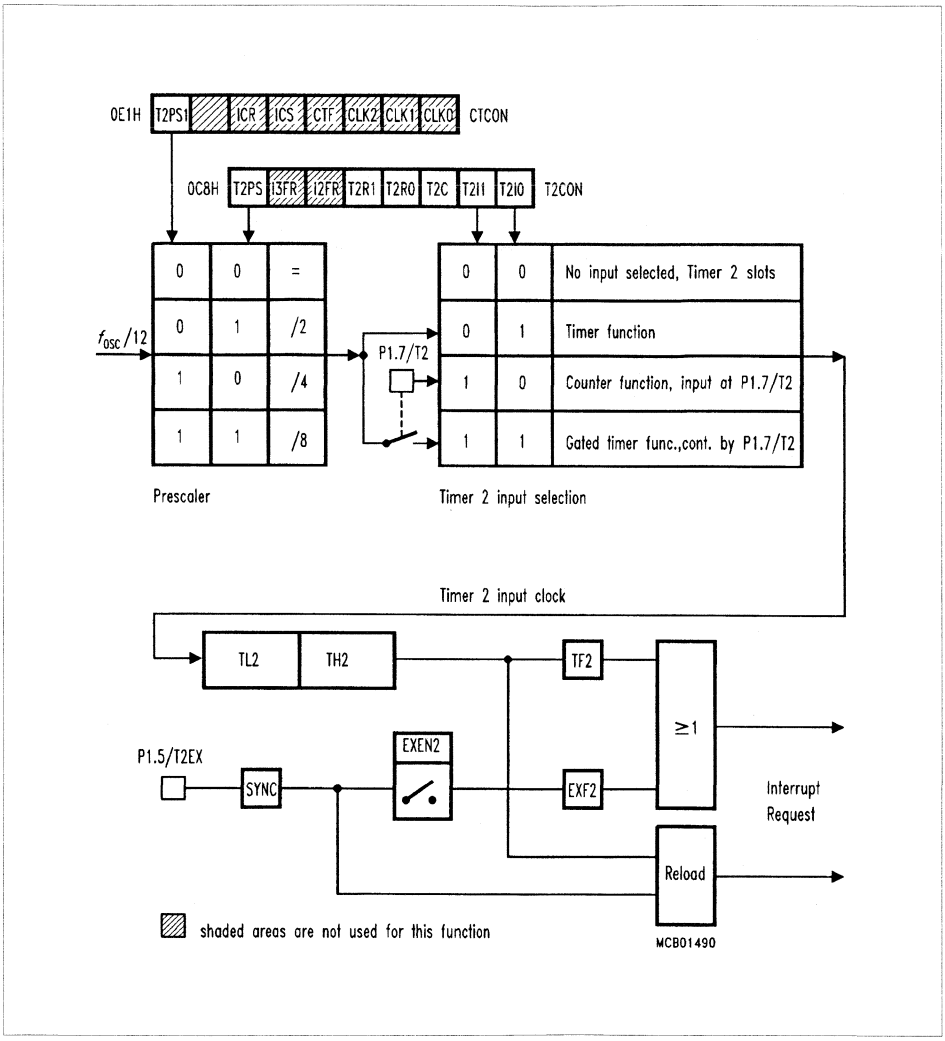


Figure 6
Block Diagram of Timer 2

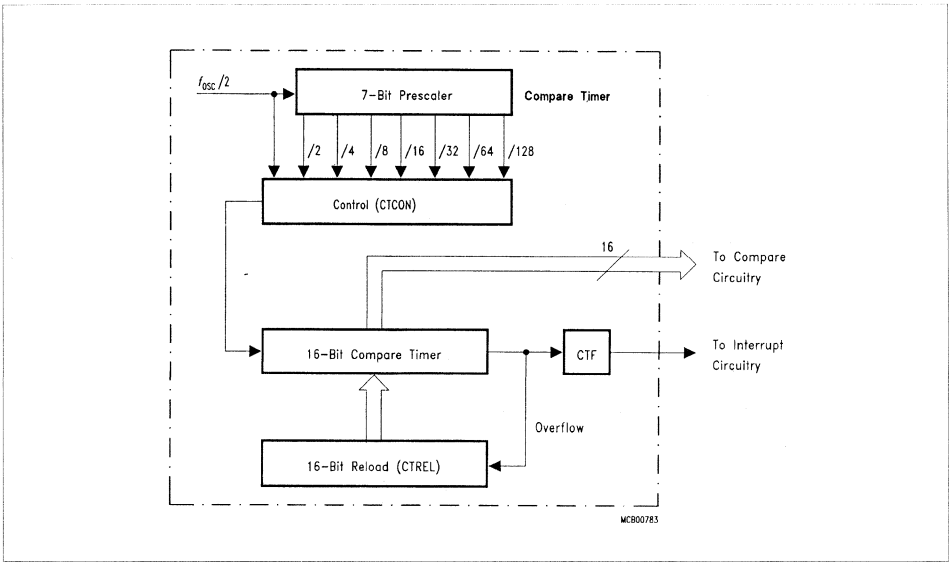


Figure 7
Block Diagram of the Compare Timer

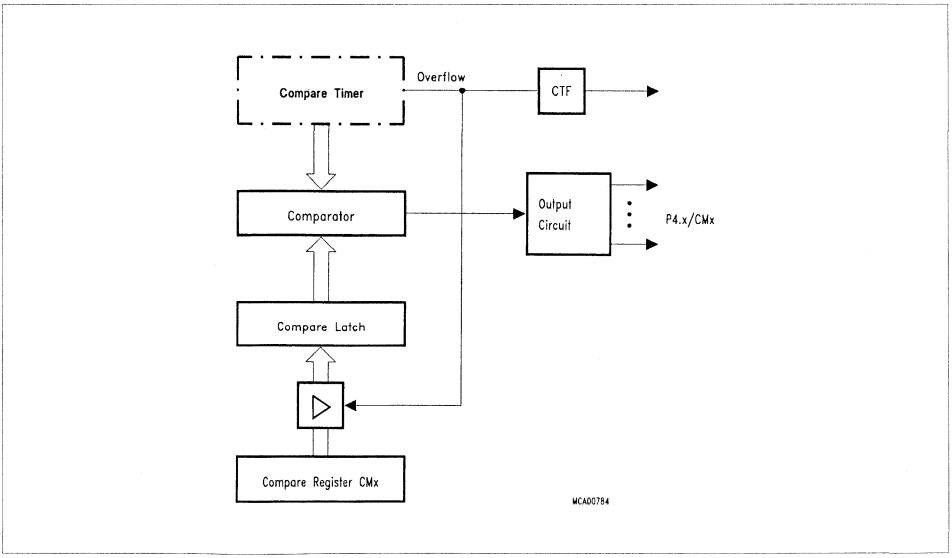


Figure 8
Compare-Mode 0 with Registers CM0 to CM7

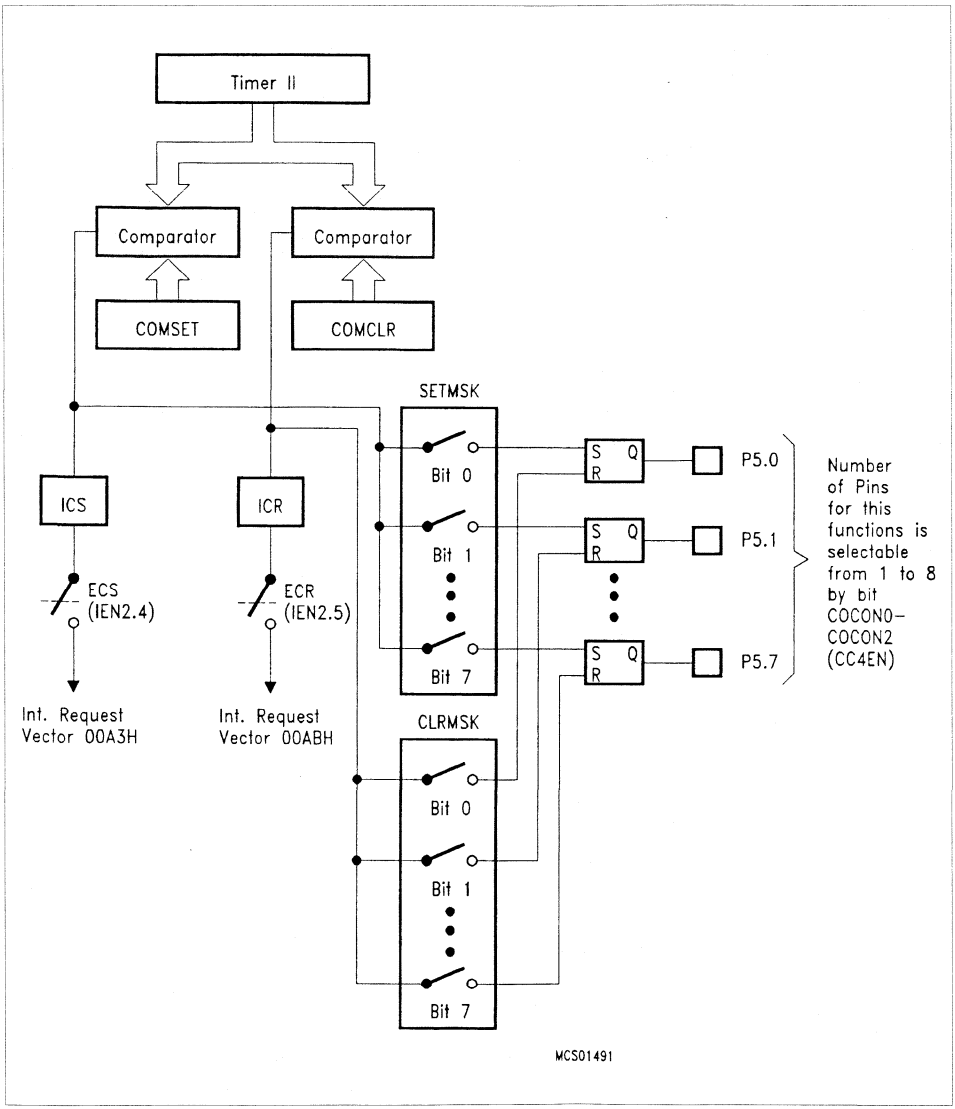


Figure 9
Compare-Mode 2 (Port 5 only)

Interrupt Structure

The SAB 80C517A has 17 interrupt vectors with the following vector addresses and request flags.

Table 5
Interrupt Sources and Vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Source
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 overflow
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 overflow
RI0 + TI0	0023H	Serial channel 0
TF2 + EXF2	002BH	Timer 2 overflow/ext. reload
IADC	0043H	A/D converter
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6
RI1/TI1	0083H	Serial channel 1
ICMP0 to ICMP7	0093H	Compare match interrupt of Compare Registers CM0-CM7 assigned to Timer 2
CTF	009BH	Compare timer overflow
ICS	00A3H	Compare match interrupt of Compare Register COMSET
ICR	00ABH	Compare match interrupt of Compare Register COMCLR

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

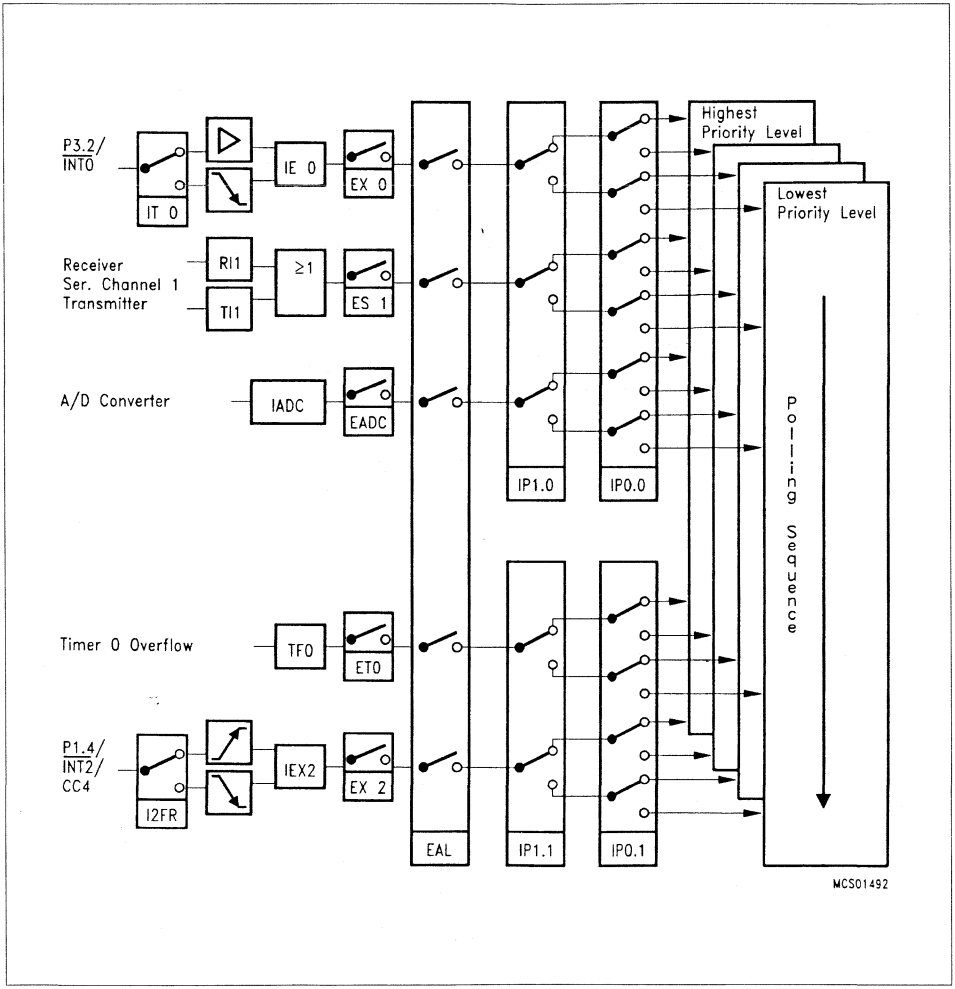


Figure 10
Interrupt Structure of the SAB 80C517A

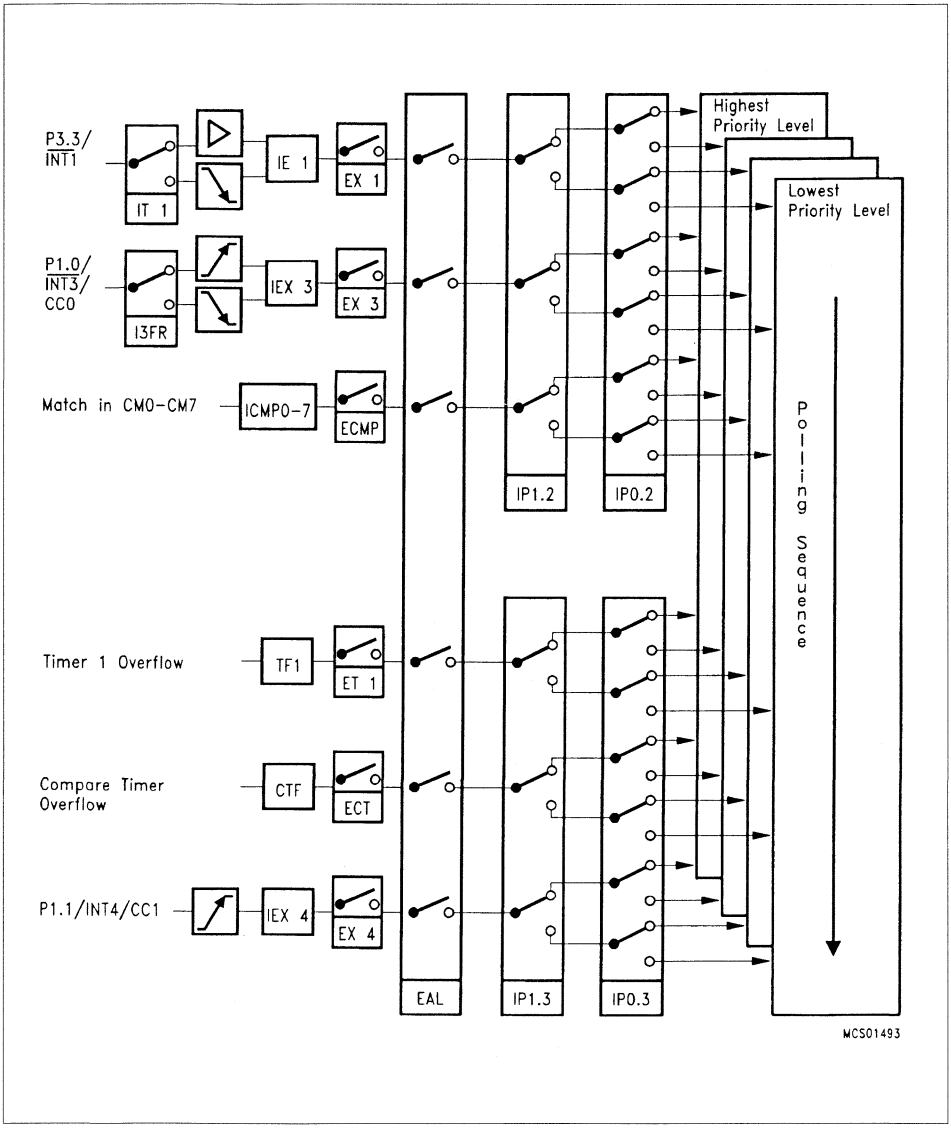


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

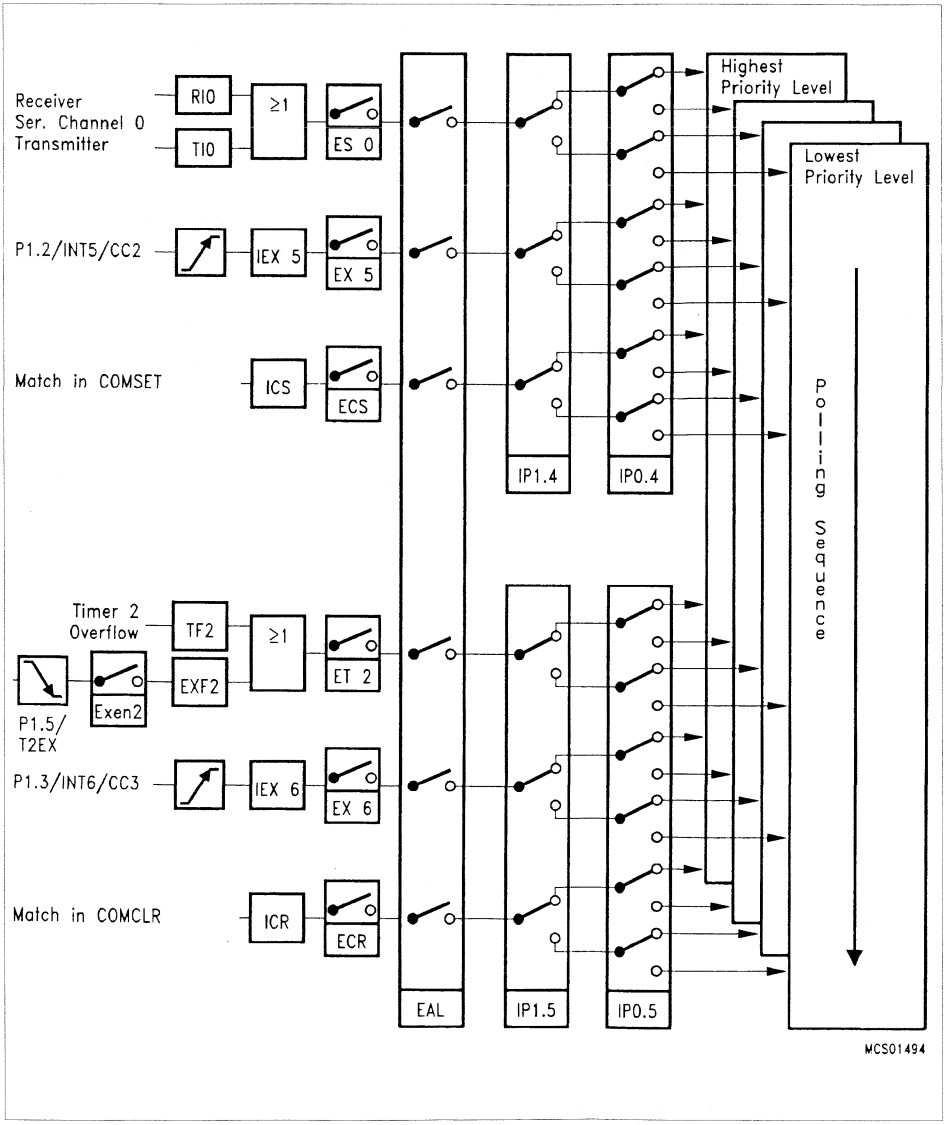


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

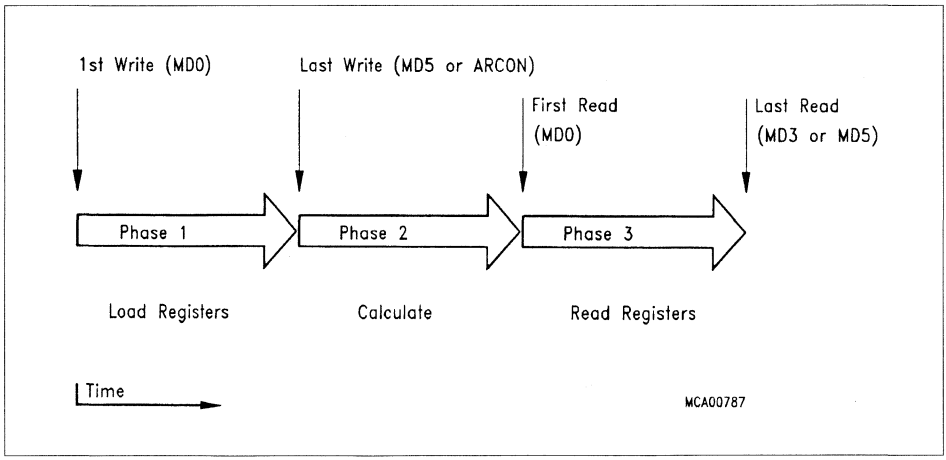
Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operation.

Operation	Result	Remainder	Execution Time
32-Bit/16-Bit	32-Bit	16-Bit	6 t_{cy} [1]
16-Bit/16-Bit	16-Bit	16-Bit	4 t_{cy}
1616-Bit *16-Bit	32-Bit	–	4 t_{cy}
32-Bit normalize	–	–	6 t_{cy} [2]
32-Bit shift left/right	–	–	6 t_{cy} [2]

[1] 1 t_{cy} = 1 µs @ 12 MHz oscillator frequency.
[2] The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:



Operation of the MDU

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

Table 6
Performing a MDU-Calculation

Operation	32-Bit/16-Bit		16-Bit/16-Bit		16-Bit * 16-Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'end	MD4	M'orL
	MD2	D'end	MD2	D'end	MD1	M'andH
	MD3	D'endH	MD3	D'endH	MD5	M'orH
	MD4	D'orL	MD4	D'orL		
Last Write	MD5	D'orH	MD5	D'orH		
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	Quo	MD1	Pr
	MD2	Quo	MD2	Quo	MD2	Pr
	MD3	QuoH	MD3	QuoH	MD3	PrH
	MD4	RemL	MD4	RemL		
Last Read	MD5	RemH	MD5	RemH		

Table 7
Shift Operation with the MDU

Operation	Normalize, Shift Left, Shift Right	
First Write	MD0	least significant byte
	MD1	
	MD2	
	MD3	most significant byte
Last Write	ARCON	start of conversion
First Read	MD0	least significant byte
	MD1	
	MD2	
Last Read	MD3	most significant byte

Abbreviations

D'end : Dividend, 1st operand of division
D'or : Divisor, 2nd operand of division
M'and : Multiplicand, 1st operand of multiplication
M'or : Multiplicator, 2nd operand of multiplication
Pr : Product, result of multiplication
Rem : Remainder
Quo : Quotient, result of division
...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

I/O Ports

The SAB 80C517A has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517A has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C517A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eighth of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.
- The **Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current.
- **The Hardware Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-Oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is independent of the state of pin $\overline{\text{PE}}$/SWD.

Hardware Enable for Software controlled Power Saving Modes

A dedicated Pin $\overline{\text{PE}}$/SWD) of the SAB 80C517A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving modes can be activated by software.

When left unconnected, Pin /$\overline{\text{PE}}$/SWD is pulled high by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. Nevertheless for a correct function of the Hardware Power Down Mode the oscillator watchdog unit including its internal RC oscillator is needed. Therefor this unit must be enabled by pin OWE (OWE = high). However, the control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software controlled power saving modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C517A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{PSEN}$ hold at logic high levels (see table 7).

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 7.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 7. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 7 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled (only if OWE = high). The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 microseconds).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases thepart from reset with oscillator watchdog status flag set.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), theWatchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal reset function. (Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	external ROM	internal ROM	external ROM	Status	Voltage range at pin
P0	Data	float	Data	float		
P1	Data alt outputs	Data alt outputs	Data last outputs	Data last outputs	floating	
P2	Data	Address	Data	Data	output	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs	
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled	$V_{SS} \leq V_{IN} \leq V_{CC}$
P5	Data alt output	Data alt output	Data last output	Data last output	input	
P6	Data alt output	Data alt output	Data last output	Data last output	function	
P7						
P8						
EA					active input	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
$\overline{PE}$/SWD					active input pull-up disabled	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
XTAL1					active output	pin may not be driven
XTAL2					disabled input functions	$V_{SS} \leq V_{IN} \leq V_{CC}$

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode (cont'd)

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	external ROM	internal ROM	external ROM	Status	Voltage range at pin
$\overline{\text{PSEN}}$					floating outp. disabled input functions	$V_{SS} \leq V_{IN} \leq V_{CC}$
ALE						
VAREF VAGND					active supply pins	$V_{AGND} \leq V_{IN} \leq V_{CC}$
OWE					active input, must be high pull-up disabl.	$V_{IN} = V_{CC}$
$\overline{\text{RESET}}$					active input must be high	$V_{IN} = V_{CC}$
$\overline{\text{RO}}$					floating output	$V_{SS} \leq V_{IN} \leq V_{CC}$

Serial Interfaces

The SAB 80C517A has two serial interfaces. Both interfaces are full duplex and receive buffered. They are functionally identical with the serial interface of the SAB 8051 when working as asynchronous channels. Serial interface 0 additionally has a synchronous mode. Table 9 shows possible configurations and the according baud rates.

Table 9
Baud Rate Generation

	Mode		**Mode 0**			–
8-Bit synchronous channel	Baudrate	f_{OSC} =1 2 MHz	1MHz			–
		f_{OSC} = 16 MHz	1.33 MHz			–
		f_{OSC} = 18 MHz	1.5 MHz			–
	derived from		f_{OSC}			–
	Mode		**Mode 1**			**Mode B**
8-Bit UART	Baudrate	f_{OSC} = 12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud	366 Baud – 375 kBaud
		f_{OSC} = 16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator	10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**		**Mode A**
9-Bit UART	Baudrate	f_{OSC} = 12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud – 75 kBaud	183 Baud – 75 kBaud
		f_{OSC}= 16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from	$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator		10-Bit Baudrate Generator

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or a dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{SMOD} * f_{OSC}}{64*(2^{10}\text{-S0REL})}$$

The default value after reset in the reload registers S0RELL and S0RELH provide a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C517.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T × D1) or received (through R × D1): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T × D1) or received (through R × D1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1.

Variable baud rates for modes A and B of serial interface 1 are derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by an 10-bit free running timer with programmable reload register.

Mode A, B baudrate = $\frac{f_{OSC}}{32 * (2^{10} - \text{SREL})}$

Watchdog Units

The SAB 80C517A offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

- programmable watchdog timer (WDT), variable from 512 µs up to appr. 1.1 s time-out period @12 MHz. Upward compatible to SAB 80515 watchdog.
- oscillator watchdog (OWD), monitors the on-chip oscillator and forces the micro-controller into reset state, in case the on-chip oscillator fails, controls the restart from the Hardware Power Down Mode and provides clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C517A then starts program execution with the WDT running. Since Pin $\overline{PE}$/SWD is only sampled during Reset (and hardware power down at parts with stepping code AD and later) dynamical switching of the WDT is not possible.

Software initialization is done by setting bit SWDT.

A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 10.

When a watchdog timer resest occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be cleared by software.

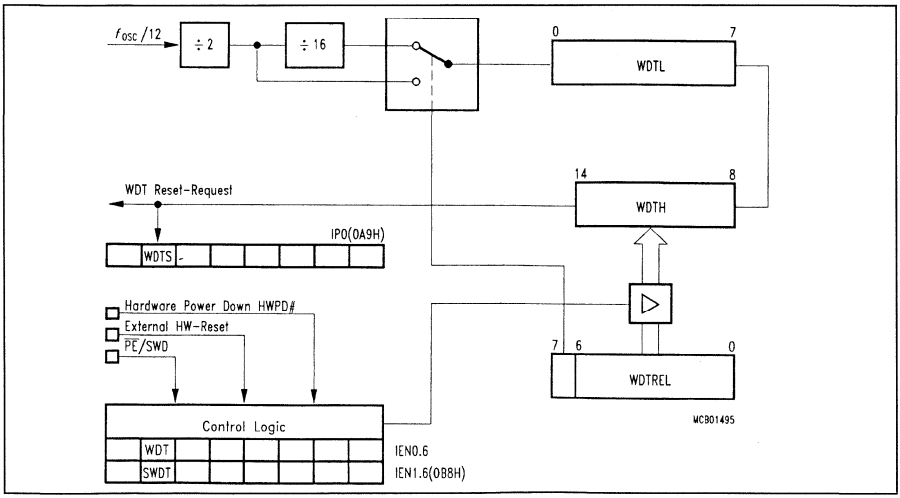


Figure 11
Block Diagram of the Programmable Watchdog Timer

Oscillator Watchdog

The unit serves three functions:

- Monitoring of the on-chip oscillator's function.
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- Restart from the Hardware Power Down Mode.
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.
- Fast internal reset after power-on.
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

If the oscillator watchdog unit is to be used it must be enabled (this is done by applying high level to the control pin OWE).

Figure 11 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency of the on-chip oscillator. The RC oscillator can be enabled/disabled by the control pin OWE. If it is disabled the complete unit has no function.

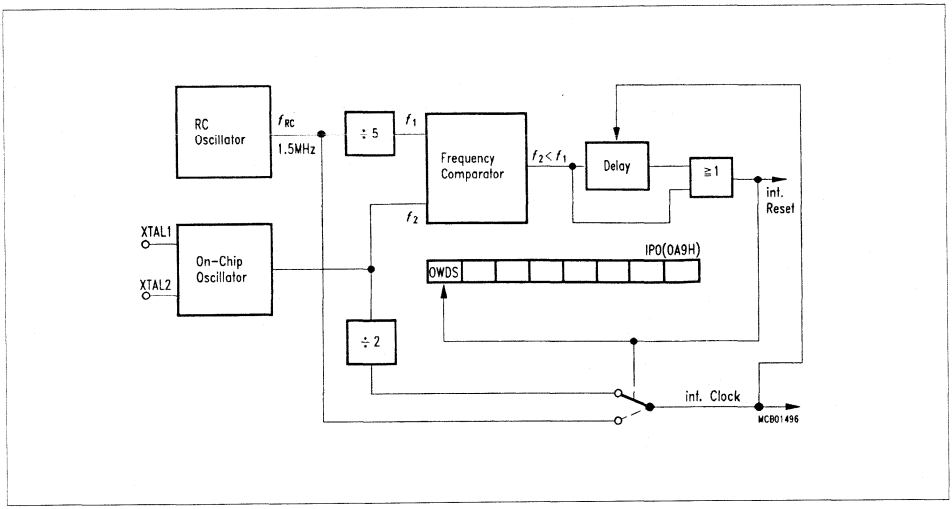


Figure 12
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C517A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C517) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C517A the oscillator watchdog unit avoids this situation. However, the oscillator watchdog must be enabled. In this case, after power-on the oscillator watch-dog's RC oscillator starts working within a very short start-up time (typ. less than 2 micro-seconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output.This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C517A / 83C517A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias ..... – 40 to 110° C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10mA to +10mA
Absolute sum of all input currents during overload condition ..... |100mA|
Power dissipation ..... 1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions (V_{IN} > V_{CC} or V_{IN} < V_{SS}) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{RESET}$, XTAL2 and $\overline{HWPD}$	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5, 6)	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1]
Output low voltage (ports ALE, $\overline{PSEN}$, RO)	V_{OL1}	–	0.45	V	I_{OL}=3.2mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–80 µA I_{OH} =–10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, RO)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–800 µA[2] I_{OH} =–80 µA[2]
Logic input low current (ports 1, 2, 3, 4, 5, 6)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, ports 7, 8, $\overline{HWPD}$)	I_{LI}	–	± 100	nA	0.45 < V_{IN} < V_{CC}
			± 150	nA	0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD, OWE)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C= 1 MHz T_A= 25 °C
Power supply current:					
Active mode, 12 MHz[7]	I_{CC}	–	28	mA	V_{CC} = 5 V,[4]
Active mode, 18 MHz[7]	I_{CC}	–	37	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz[7]	I_{CC}	–	24	mA	V_{CC} = 5 V,[5]
Idle mode, 18 MHz[7]	I_{CC}	–	31	mA	V_{CC} = 5 V,[5]
Slow down mode, 12 MHz	I_{CC}	–	12	mA	V_{CC} = 5 V,[6]
Slow down mode, 18MHz	I_{CC}	–	16	mA	V_{CC} = 5 V,[6]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2...5.5 V, [3]

Notes see page 341.

Notes for page 340:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power down mode) is measured with:
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = OWE = V_{SS}; $\overline{HWDP}$ = V_{CC} (Software Power Down mode); V_{AREF} = V_{CC};
V_{AGND} = V_{SS}; all other pins are disconnected. Hardware Powerdown I_{PD} : OWE = V_{CC} or V_{SS}. No certain pin connection for the other pins.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS}
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V;
XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; HWPD = V_{CC}; Port0 = Port7 = Port8 = V_{CC} ;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V;
XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port7 = Port8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS} ;
all other pins are disconnected;

7) $I_{CC\,Max}$ at other frequencies is given by:
active mode: I_{CC} (max) = 1.50* f_{OSC} + 10
idle mode: I_{CC} (max) = 1.17* f_{OSC} + 10
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
$V_{AREF} = V_{CC} \pm 5\%$; $V_{AGND} = V_{SS} \pm 0.2$ V;
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 ° C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY} [1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	$V_{AREF} = V_{CC}$ $V_{AGND} = V_{SS}$
V_{AREF} supply current	I_{REF}		± 20		µA	[4]

[1] $t_{CY} = (8*2^{ADCL}) / f_{OSC}$; ($t_{CY} = 1/f_{ADC}$; $f_{ADC} = f_{OSC}/(8*2^{ADCL})$)
[2] This parameter specifies the time during the input capacitance C_I can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
[3] This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.
[4] The differencial impedance r_D of the analog reference source must be less than 1 KΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to110 ° C for the SAB 80C517A-T4/83C517A-5-T4

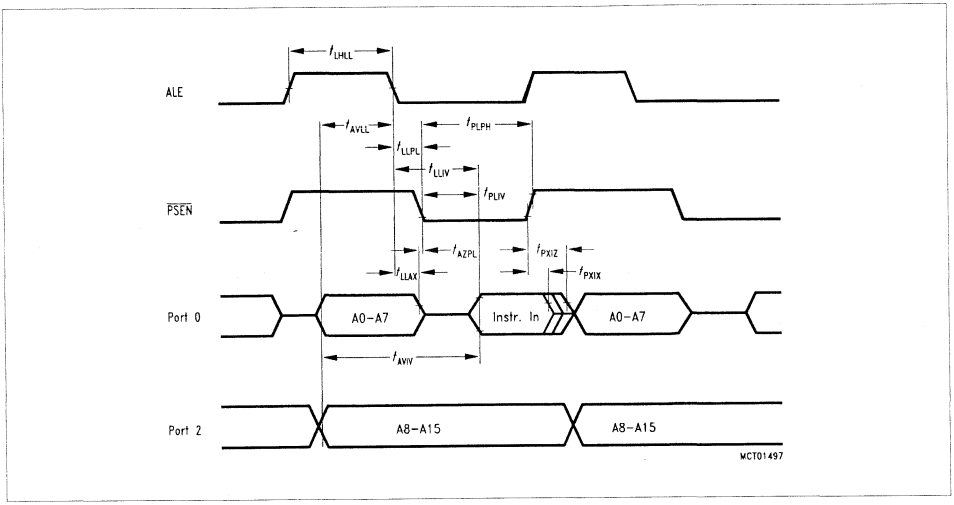
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	71	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	26	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	26	–	$t_{CLCL} - 30$	–	ns
Address to valid instruction	t_{LLIV}	–	122	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction	t_{PLIV}	–	92	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	46	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	48	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	218	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

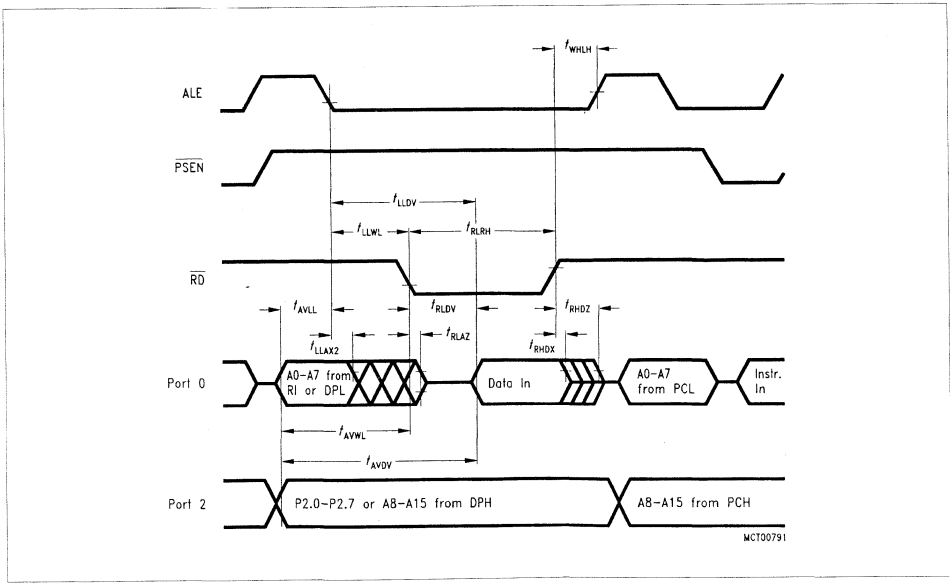
*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

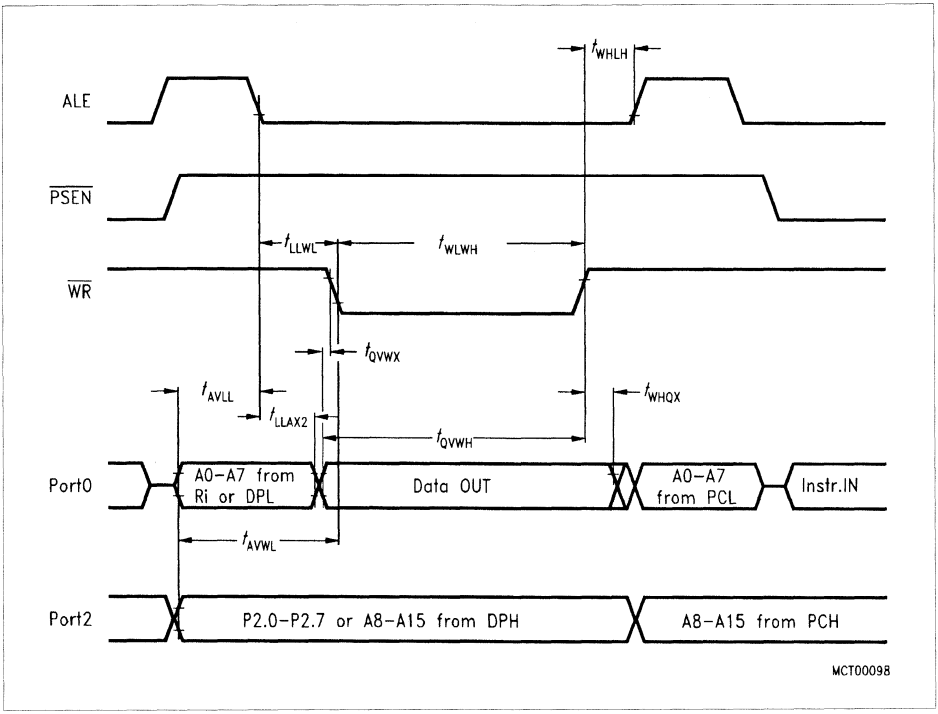
Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



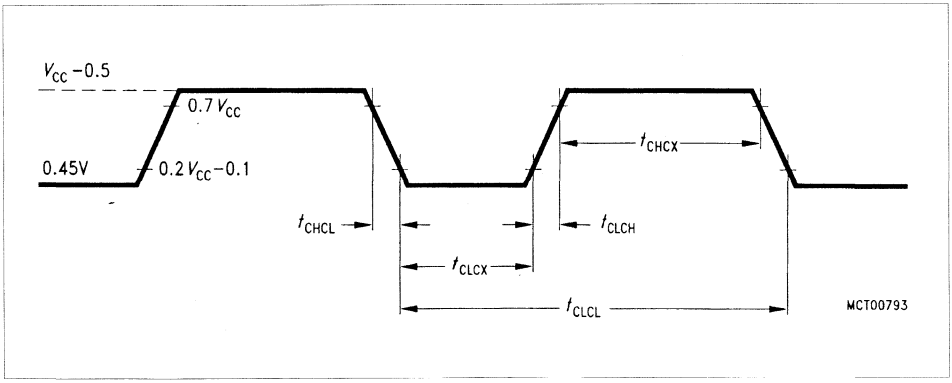
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

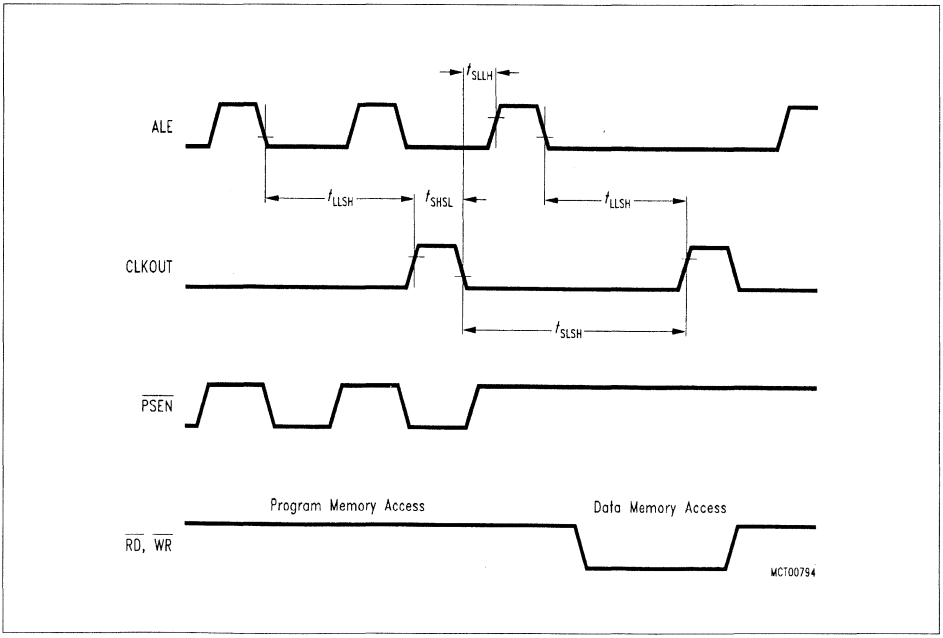
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 18 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	285	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	3.5	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	$7\ t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	71	–	$2\ t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	516	–	$10\ t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



System Clock Timing

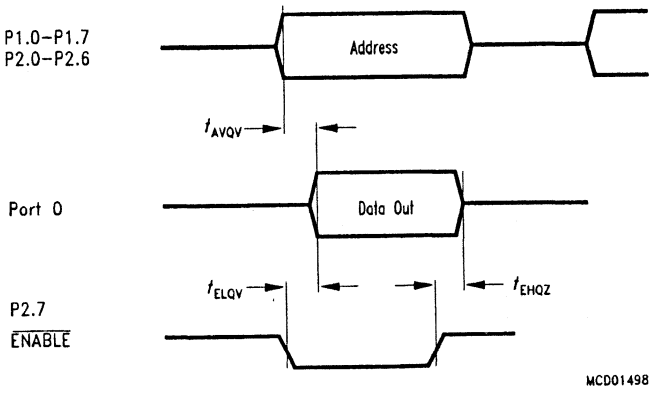
ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	

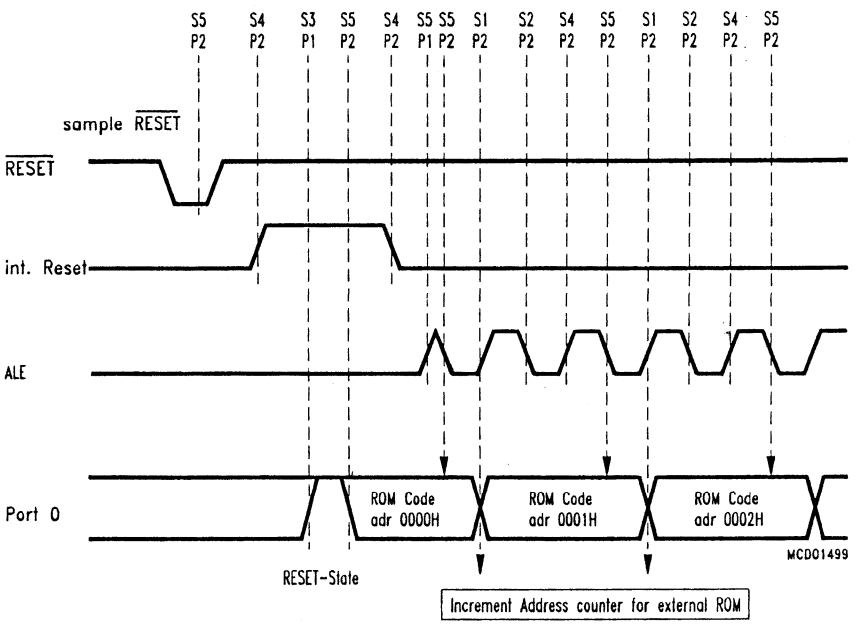
ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



ROM Verification Mode 1

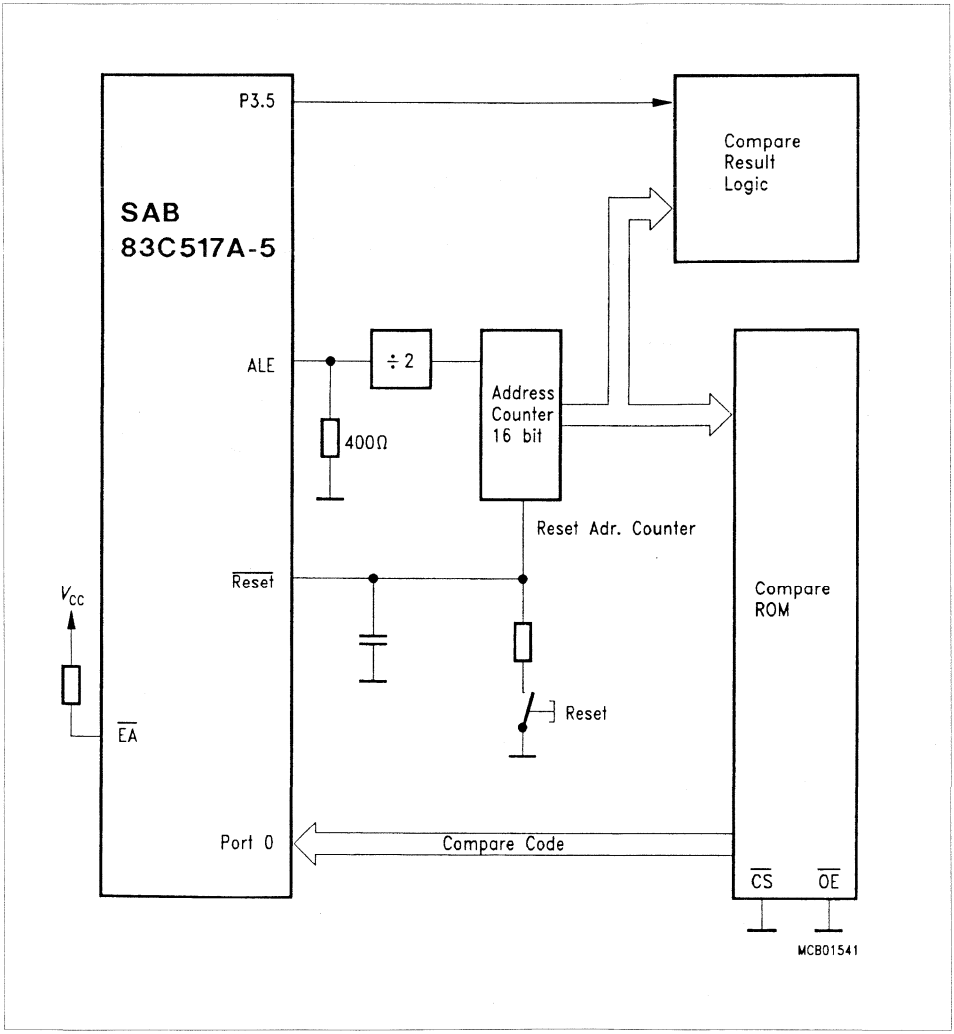
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



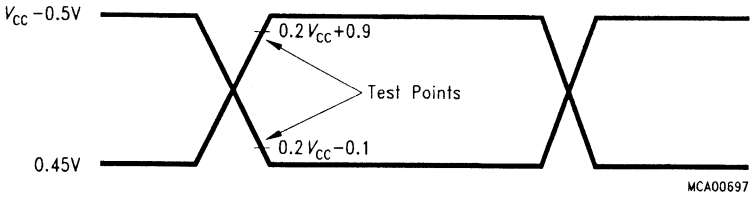
Inputs $\overline{EA}= V_{IH}$
ALE forced to low level by a weak pull down resistor (approx.400Ω),
durind $\overline{RESET}$ activ ROM-Code: Port 0=D0-D7

Outputs Port 3.5 shows all 1024 cycles low level for one cycle
when compared ROM-Code was not allright

ROM Verification Mode 2

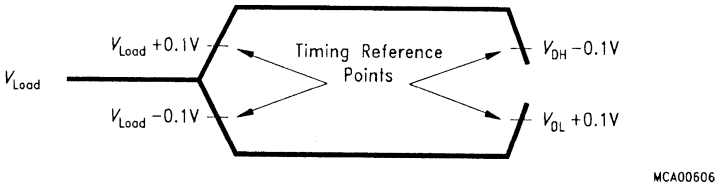


Application Circuitry for Verifying the Internal ROM



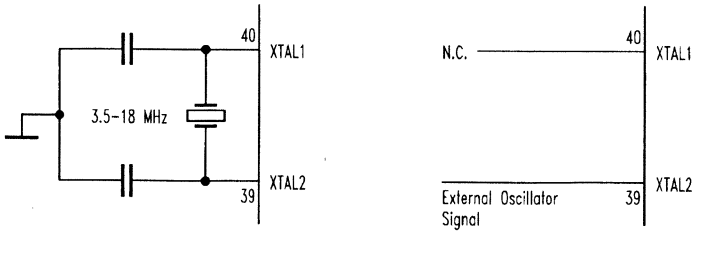
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



Recommended Oscillator Circuits

SIEMENS

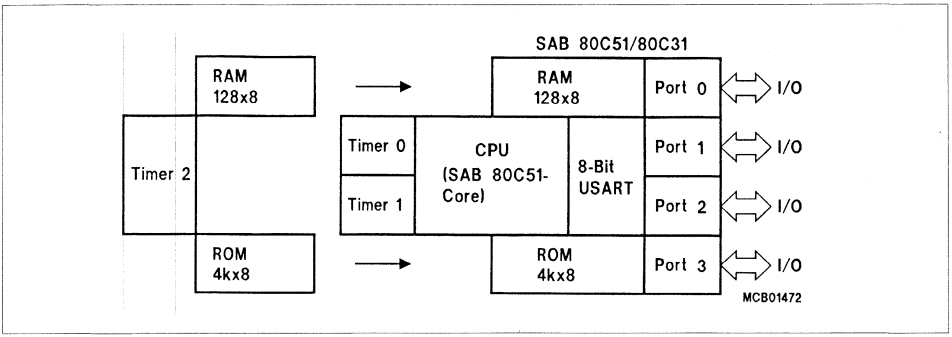
High-Performance 8-Bit CMOS Microcontroller

SAB 80C52/80C32

Preliminary

SAB 80C52	CMOS microcontroller with factory-maskprogrammable ROM
SAB 80C32	CMOS microcontroller for external ROM

- Versions for 12 MHz /16MHz /20 MHz operating frequency
- 8 K × 8 ROM (SAB 80C52 only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs /750 ns /666 ns
- Multiply and divide in 4 µs /3 µs /2.7 µs
- Six interrupt sources, two priority levels
- Idle and power-down operation
- Fully functionally compatible with SAB 8052A/8032A
- Three temperature ranges available:
  0t o 70°C,
  – 40 to +85°C,
  – 40 to +110°C
- P-DIP-40 and P-LCC-44 package



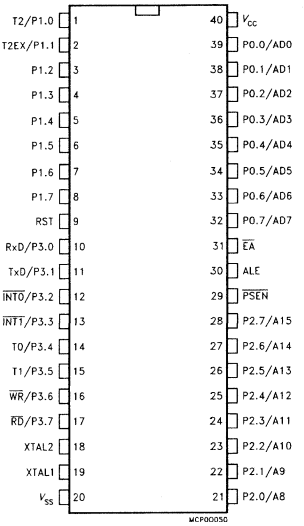
The SAB 80C52/80C32 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8052A/ 8032A devices in MYMOS technology.

Furthermore, it is backwardly compatible with the SAB 80C51/80C31. The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C52/80C32 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

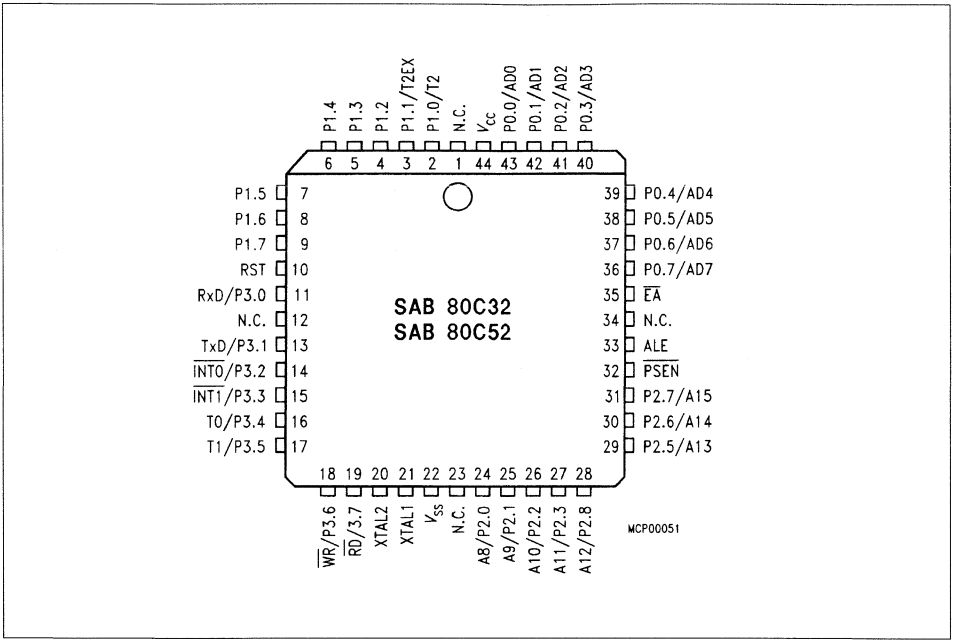
The SAB 80C52 contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 K × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C32 is identical, except that it lacks the program memory on the chip.

Ordering Information

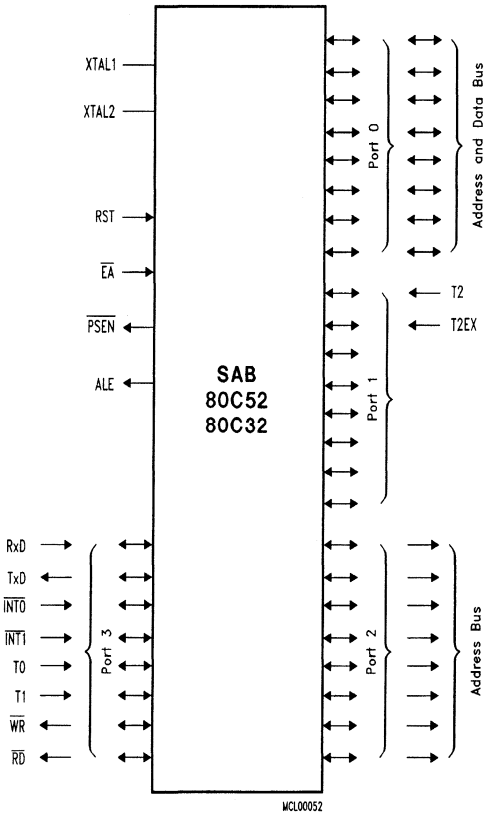
Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C52-N SAB 80C52-P	Q67120-C396 Q67120-C379	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz
SAB 80C32-N SAB 80C32-P	Q67120-C395 Q67120-C378	P-LCC-44 P-DIP-40	for external memory,12 MHz
SAB 80C52-P-T40/85	Q67120-C521	P-DIP-40	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C32-P-T40/85	Q67120-C520	P-DIP-40	for external memory, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C52-16-N SAB 80C52-16-P	Q67120-C503 Q67120-C501	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 16 MHz
SAB 80C32-16-N SAB 80C32-16-P	Q67120-C502 Q67120-C500	P-LCC-44 P-DIP-40	for external memory, 16 MHz
SAB 80C52-16-P-T40/85	Q67120-C563	P-DIP-40	with factory mask-programmable ROM, 16 MHz, ext. temp. – 40 to 85 °C
SAB 80C32-16-P-T40/85	Q67120-C527	P-DIP-40	for external memory,16 MHz ext. temp. -40 to 85 °C
SAB 80C52-20-N SAB 80C52-20-P	Q67120-C710 Q67120-C708	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz
SAB 80C32-20-N SAB 80C32-20-P	Q67120-C711 Q67120-C709	P-LCC-44 P-DIP-40	for external memory, 20 MHz



Pin Configuration
(P-DIP-40)



Pin Configuration
(P-LCC-44)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-DIP-40	P-LCC-44		
P1.0-P1.7	1-8	2-9	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0): Input to counter 2. – T2 EX (P1.1): Capture/Reload trigger of timer 2.
RST	9	10	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-DIP-40	P-LCC-44		
P3.0-P3.7	10-17	11, 13-19	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R x D/data (P3.0): Serial port's receiver data input (asynchronous) or data input/output (synchronous). – T x D/clock (P3.1): Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2): Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3): Interrupt 1 input or gate control input for counter 1. – T0 (P3.4): Input to counter 0. – T1 (P3.5): Input to counter 1. – $\overline{WR}$ (P3.6): The write control signal latches the data byte from port 0 into the external data memory. – (P3.7): The read control signal enables external data memory to port 0.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-DIP-40	P-LCC-44		
XTAL1 XTAL2	19 18	21 20	I/O	**XTAL 1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL 2** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.
P2.0-P2.7	21-28	24-31	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resist. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-DIP-40	P-LCC-44		
$\overline{\text{PSEN}}$	29	32	O	**$\overline{\text{Program Store Enable}}$** This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	**Address Latch Enable** Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	31	35	I	**$\overline{\text{External Access}}$** When held at a high level, the SAB 80C52 executes instructions from the internal ROM when the PC is less than 8192. When held at a low level, the SAB 80C52 fetches all instructions from the external program memory. For the SAB 80C32 this pin must be tied low.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-DIP-40	P-LCC-44		
				Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C52. External pullup resistors are required during program verification.
V_{CC}	40	44		**Supply voltage** during normal, idle, and power-down operations.
V_{SS}	20	22		**Circuit ground potential**.
NC	–	1, 12, 23, 24	–	**No connection**.

* I = Input
O = Output

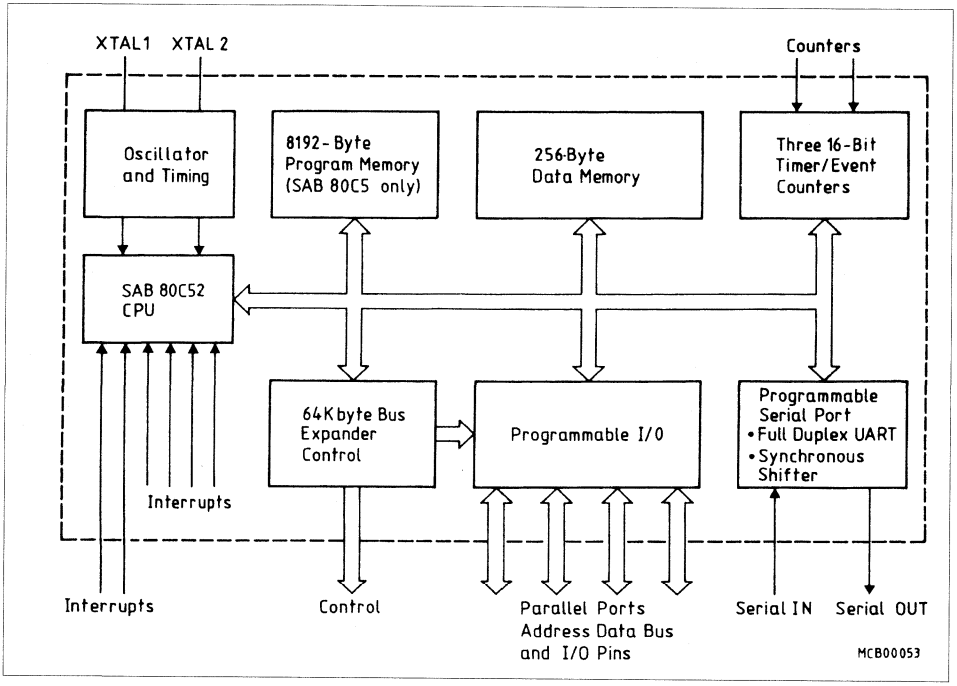


Figure 1
Block Diagram

Functional Description

The SAB 80C52/80C32 is functionally compatible with the SAB 8052A/8032A products that are designed in Siemens MYMOS technology. Furthermore, the SAB 80C52/80C32 is backwardly compatible with the SAB 80C51/80C31 devices.

In addition, instead of the RAM backup power supply of the SAB 8052A/8032A, the SAB 80C52/ 80C32 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

Idle mode

In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardwarere set which starts the processor in the same way as a power-on reset.

Power-down mode

In the power-down mode the oscillator is stopped, and the instruction that invoke power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data/ Alternate Outputs	Data	Data/ Alternate Outputs
Idle	External	1	1	Float	Data/ Alternate Outputs	Address	Data/ Alternate Outputs
Power-Down	Internal	0	0	Data	Data/ Last Output of Alternate Function	Data	Data/ Last Output of Alternate Function
Power-Down	External	0	0	Float	Data/ Last Output of Alternate Function	Data	Data/ Last Output of Alternate Function

Instruction Set

The SAB 80C52/80C32 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function

Register, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-B6229-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to 70 °C (SAB 80C52/80C32)
– 40 to 85 °C (SAB 80C52/80C32-T40/85)
– 40 to 110 °C (SAB 80C52/80C32-T40/110)
Storage temperature ..... – 65 to 150 °C
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} 0.5 V
Voltage on V_{CC} to V_{SS} ..... – 0.5 to 6.5 V
Power dissipation ..... 1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V; T_A = 0 to 70 °C (SAB 80C52/80C32)
T_A = – 40 to 85 °C (SAB 80C52/80C32-T40/85)
T_A = – 40 to 110 °C (SAB 80C52/80C32-T40/110)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$) for SAB 80C52/80C32, 80C52/80C32-T40/85 for SAB 80C52/80C32, T40/110	V_{IL}	 – 0.5 – 0.5	 0.2 V_{CC} – 0.1 0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input high voltage (except XTAL1, RST)	V_{IH}	0.2 V_{CC} + 0.9	0.2 V_{CC} + 0.5	V	–
Input high voltage (XTAL1, RST)	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 V_{CC} 0.9	–	V	I_{OH} = – 80 µA I_{OH} = – 10 µA

Notes see page 369

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$	V_{OH1}	2.4 V_{CC} 0.9	– –	V V	I_{OL} = – 800 µA I_{OL} = – 80 µA [2]
Logical 0 input current (ports 1, 2, 3)	I_{IL}	–	– 50	V	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	–	– 650	V V	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 10	µA	0.45 < V_{IN} < V_{CC}
Reset pulldown resistor	R_{RST}	40	150	kΩ	–
Pin capacitance	C_{IO}	–	10		f < = 1 MHz, T_A = 25 °C
Power supply current: Active mode, 12 MHz [6] Active mode, 16 MHz [6] Idle mode,12 MHz [6] Idle mode,16 MHz [6] Power Down Mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 – – – – –	 20 26 6.8 8.4 50	 mA mA mA mA µA	 V_{CC} = 5 V [4] V_{CC} = 5 V [4] V_{CC} = 5 V [5] V_{CC} = 5 V [5] V_{CC} = 2...5.5 V [3]

Notes see page 369

Notes for pages 367 and 368

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = V_{CC}; XTAL1 = V_{SS}; XTAL2 = N.C.;

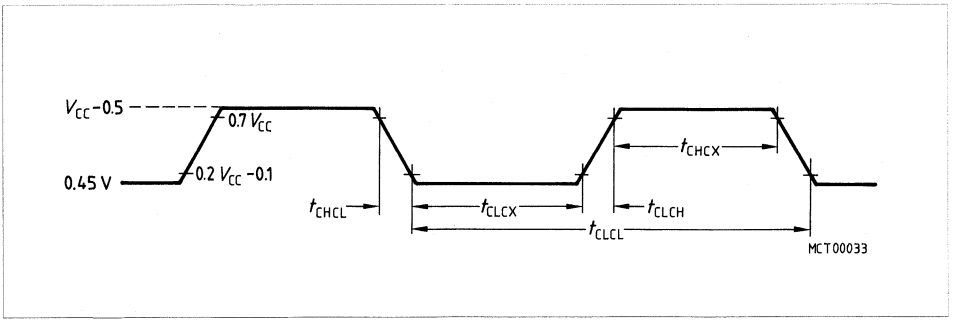
4) I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{CC}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = V_{CC}; RST = V_{SS}; all other pins are disconnected.

6) $I_{CC\ Max}$ at other frequencies is given by:

   active mode: $I_{CC\ Max} = 1.5 * f_{OSC} + 2.0$
   idle mode: $I_{CC\ Max} = 0.4 * f_{OSC} + 2.0$

   where f_{OSC} is the oscillator frequency im MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V (see also notes 5 and 6)



Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode

AC Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
T_A = 0 to 70 °C; (SAB 80C52/80C32)
T_A = – 40 to 85 °C; (SAB 80C52/80C32 – T40/85)
T_A = – 40 to 110 °C; (SAB 80C52/80C32 – T40/110)
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	60	–	$t_{CLCL} - 23$	–	ns
Address to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instruction in	t_{AVIV}	–	302	0	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{PLAZ}	–	0	–	0	ns

*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWX}	433	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 12 MHz		
		min	max.	
External Clock Drive XTAL1				
Oscillator period	t_{CLCL}	83.3	2000	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics (cont'd)

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
T_A = 0 to 70 °C; (SAB 80C52-16/80C32-16)
T_A = – 40 to 85 °C; (SAB 80C52-16/80C32-16 – T40/85)
T_A = – 40 to 110 °C; (SAB 80C52-16/80C32-16 – T40/110)
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 16 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	23	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	40	–	$t_{CLCL} - 23$	–	ns
Address to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	63	–	$t_{CLCL} - 15$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	60	–	$t_{CLCL} - 3$	–	ns
Address to valid instruction in	t_{AVIV}*)	–	302	0	$5t_{CLCL} - 90$	ns
Address float to $\overline{PSEN}$	t_{PLAZ}	–	0	–	0	ns

*) Interfacing the SAB 80C52-16/80C32-16 to devices with float times up to 45 ns permissible. This limited bus contention will not cause any damage to port 0 drivers

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 16 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWX}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 16 MHz		
		min	max.	
External Clock Drive XTAL1				
Oscillator period	t_{CLCL}	62.5	2000	ns
High time	t_{CHCX}	15	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	15	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns

AC Characteristics (cont'd)

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
T_A = 0 to 70 °C; (SAB 80C52-20/80C32-20)
T_A = – 40 to 85 °C; (SAB 80C52-20/80C32-20 – T40/85)
T_A = – 40 to 110 °C; (SAB 80C52-20/80C32-20 – T40/110)
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		20 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 20 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	60	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
Address to valid instruction in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instruction in	t_{AVIV}*)	–	190	0	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{PLAZ}	–	10	–	0	ns

*) Interfacing the SAB 80C52-20/80C32-20 to devices with float times up to 45 ns permissible. This limited bus contention will not cause any damage to port 0 drivers

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		20 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 MHz to 20 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	200	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	65	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	85	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	40	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	250	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	285	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	4 t_{CLCL} – 130	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	t_{CLCL} – 30	t_{CLCL} + 30	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWX}	200	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

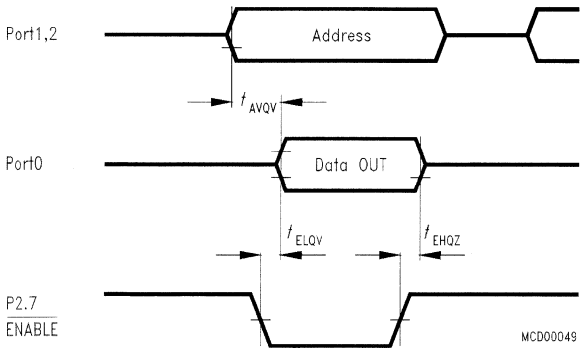
AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 0.5 MHz to 20 MHz		
		min	max.	
External Clock Drive XTAL1				
Oscillator period	t_{CLCL}	50	2000	ns
High time	t_{CHCX}	12	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	12	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	
ROM Verification				
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
$\overline{\text{ENABLE}}$ to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

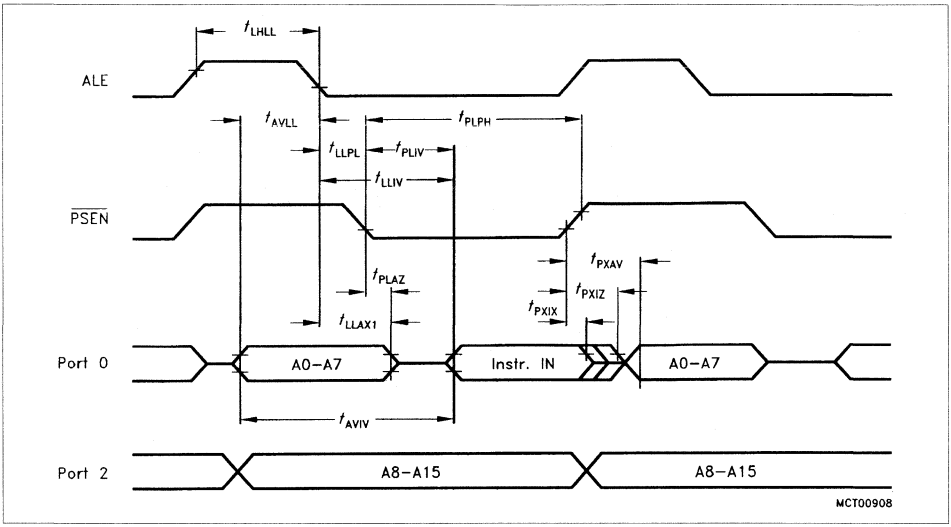


Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12
Data: Port 0 = D0–D7

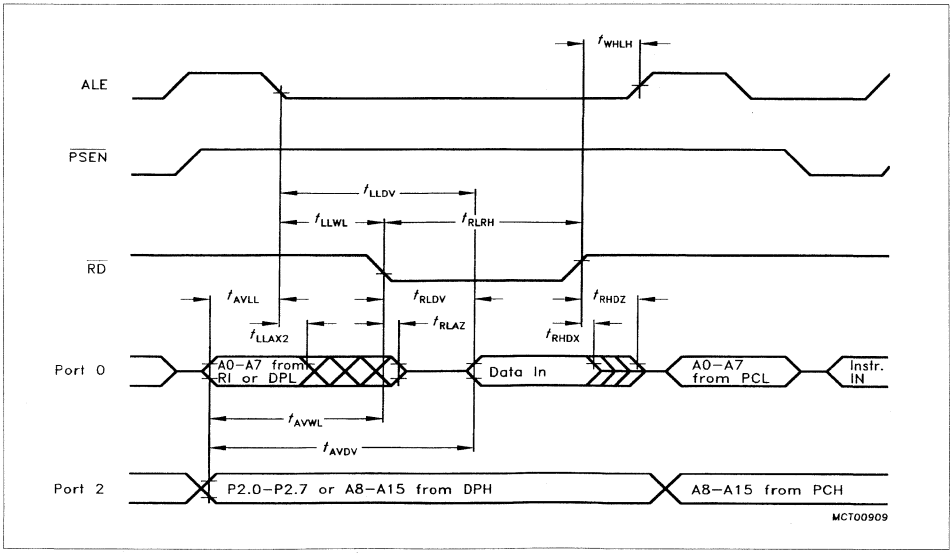
Inputs: P2.5–P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
RST = V_{IH1}

ROM Verification

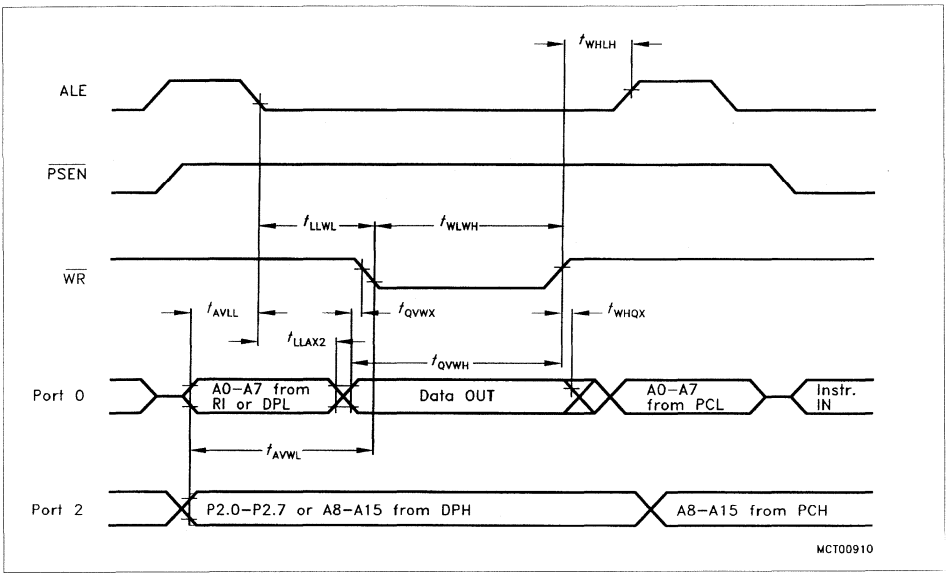
Waveforms



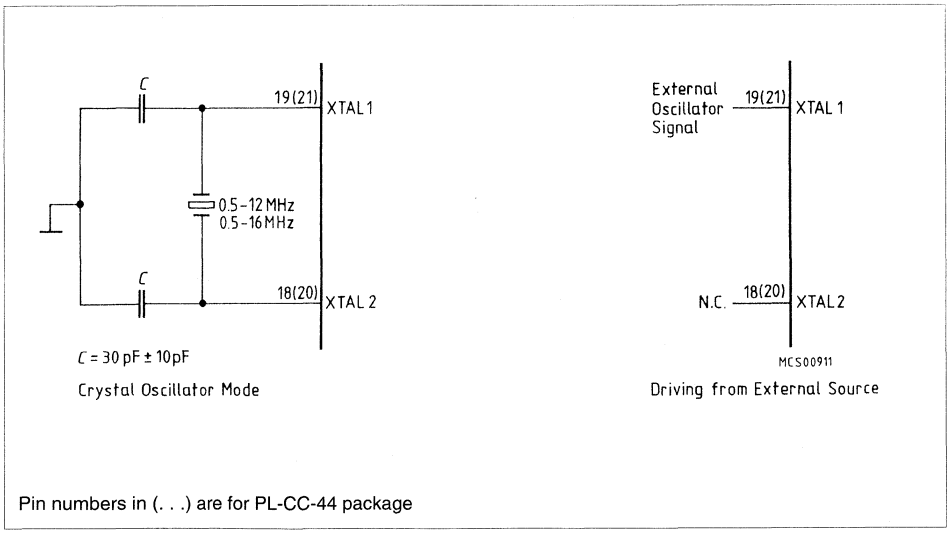
Program Memory Read Cycle



Data Memory Read Cycle

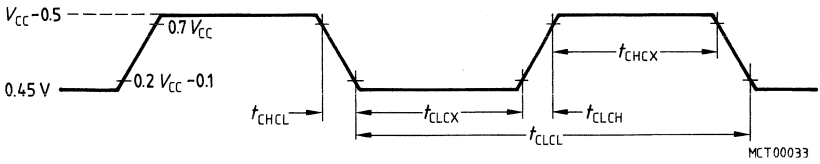


Data Memory Write Cycle

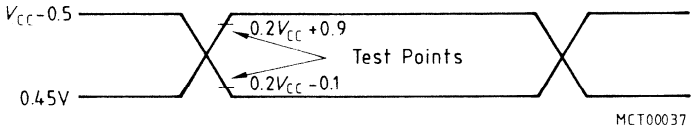


Pin numbers in (. . .) are for PL-CC-44 package

Recommended Oscillator Circuits

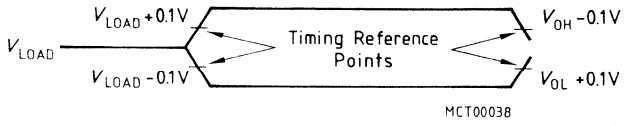


External Clock Cycle



AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms

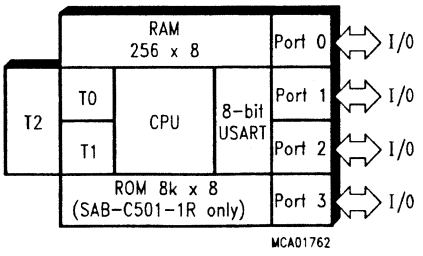
SIEMENS

8-Bit CMOS Microcontroller — SAB-C501

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12/20/40 MHz operating frequency
- 8 K × 8 ROM (SAB-C501-1R only)
- 256 × 8 RAM
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- P-DIP-40 and P-LCC-44 package
- Temperature ranges: SAB-C501 T_A: 0 °C to 70 °C
  SAF-C501 T_A: – 40 °C to 85 °C

SAB-C501



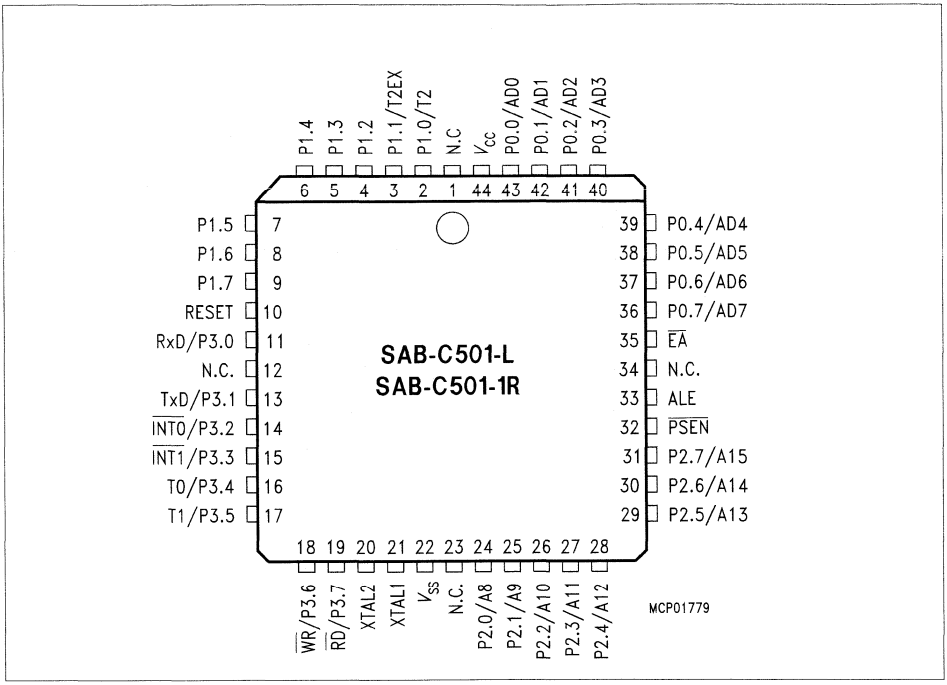
The SAB-C501-L/C501-1R described in this document is compatible with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

The SAB-C501-1R contains a non-volatile 8K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers counters, a seven source, two priority level interrupt structure and a serial port. The SAB-C501-L is identical, except that it lacks the program memory on chip. Therefore the term SAB-C501 refers to both versions within this specification unless otherwise noted.

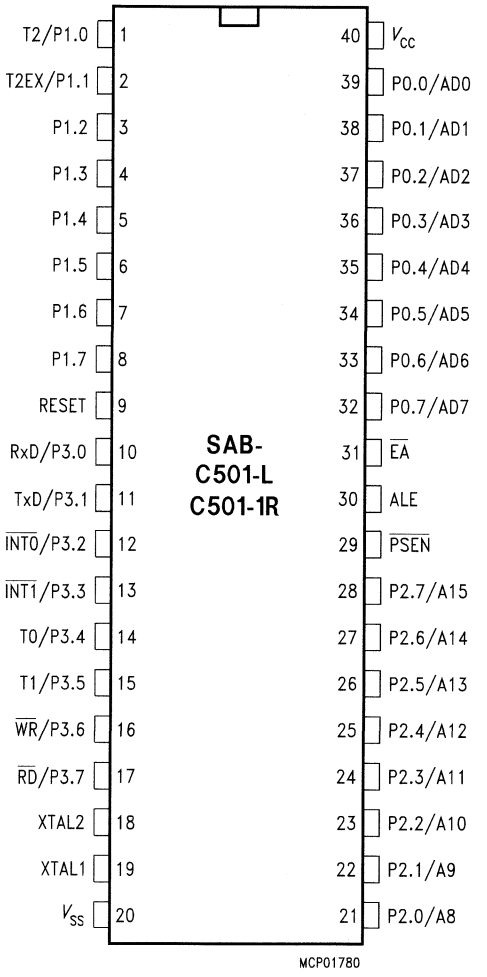
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501-LN SAB-C501-LP	Q67120-C844 Q67120-C846	P-LCC-44 P-DIP-40	for external memory 12 MHz
SAB-C501-1RN SAB-C501-1RP	Q67120-C840 Q67120-C842	P-LCC-44 P-DIP-40	with factory mask-programmable ROM 12 MHz
SAB-C501-L20N SAB-C501-L20P	Q67120-C865 Q67120-C866	P-LCC-44 P-DIP-40	for external memory 20 MHz
SAB-C501-1R20N SAB-C501-1R20P	Q67120-C873 Q67120-C874	P-LCC-44 P-DIP-40	with factory mask-programmable ROM 20 MHz
SAB-C501-L40N SAB-C501-L40P	Q67120-C867 Q67120-C868	P-LCC-44 P-DIP-40	for external memory 40 MHz
SAB-C501-1R40N SAB-C501-1R40P	Q67120-C875 Q67120-C876	P-LCC-44 P-DIP-40	with factory mask-programmable ROM 40 MHz
SAF-C501-LN SAF-C501-LP	Q67120-C845 Q67120-C847	P-LCC-44 P-DIP-40	for external memory, 12 MHz ext. temp. – 40 °C to 85 °C
SAF-C501-1RN SAF-C501-1RP	Q67120-C841 Q67120-C843	P-LCC-44 P-DIP-40	with factory mask-programmable ROM 12 MHz ext. temp. – 40 °C to 85 °C
SAF-C501-L20N SAF-C501-L20P	Q67120-C870 Q67120-C869	P-LCC-44 P-DIP-40	for external memory, 20 MHz ext. temp. – 40 °C to 85 °C
SAF-C501-1R20N SAF-C501-1R20P	Q67120-C871 Q67120-C872	P-LCC-44 P-DIP-40	with factory mask-programmable ROM 20 MHz ext. temp. – 40 °C to 85 °C

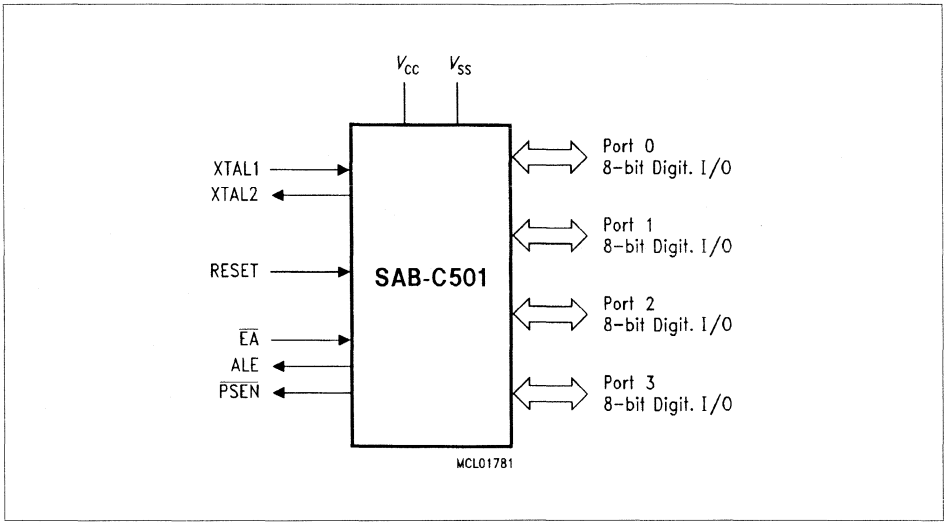
Note: Extended temperature range – 40 °C to 110 °C (SAH-C501) on request.



Pin Configuration
(P-LCC-44)



Pin Configuration
(P-DIP-40)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P1.7 – P1.0	9–2	8–1	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: P1.0 T2 Input to counter 2 P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count
	2	1		
	3	2		

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P3.0 – P3.7	11, 13–19	10–17	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10		P3.0 RxD receiver data input (asynchronous) or data input output (synchronous) of serial interface 0
	13	11		P3.1 TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12		P3.2 $\overline{\text{INT0}}$ interrupt 0 input/timer 0 gate control
	15	13		P3.3 $\overline{\text{INT1}}$ interrupt 1 input/timer 1 gate control
	16	14		P3.4 T0 counter 0 input
	17	15		P3.5 T1 counter 1 input
	18	16		P3.6 $\overline{\text{WR}}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17		P3.7 $\overline{\text{RD}}$ the read control signal enables the external data memory to port 0
XTAL2	20	18	–	**XTAL2** Output of the inverting oscillator amplifier.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
XTAL1	21	19	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	I/O	**Port 2** ia a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	O	**The Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
RST	10	9	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE	33	30	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.
$\overline{EA}$	35	31	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB C501-1R only) when the PC is less than 2000_H. When held at low level, the SAB C501 fetches all instructions from external program memory. For the SAB C501-L this pin must be tied low.
P0.0 – P0.7	43–36	39–32	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB C501-1R. External pull-up resistors are required during program verification.
V_{SS}	22	20	–	**Circuit ground potential**
V_{CC}	44	40	–	**Supply terminal** for all operating modes
N.C.	1, 12, 23, 24	–	–	**No connection**

*) I = Input
O = Output

Functional Description

The SAB-C501 is fully compatible to standard 8051 microcontroller family.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52 the SAB-C501 incorporates some enhancements in the Timer2 Unit.

Figure 1 shows a block diagram of the SAB-C501.

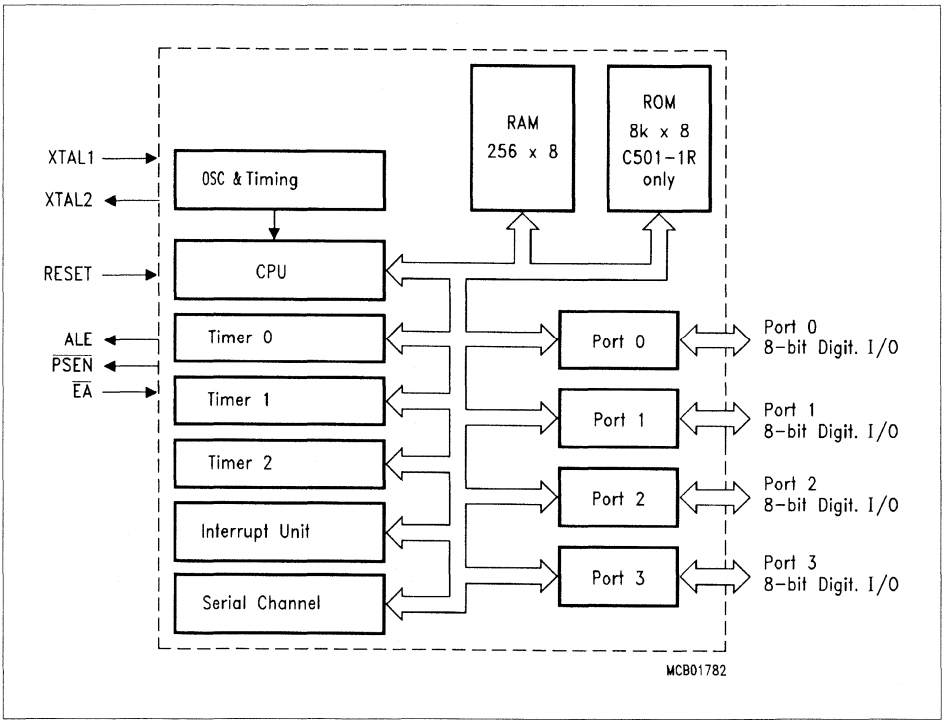


Figure 1, Block Diagram of the SAB-C501

CPU

The SAB-C501 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions are executed in 1.0 µs (20 MHz: 600 ns, 40 MHz : 300 ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $0D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxilliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address $00_H - 07_H$
0	1	Bank 1 selected, data address $08_H - 0F_H$
1	0	Bank 2 selected, data address $10_H - 17_H$
1	1	Bank 3 selected, data address $18_H - 1F_H$
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag** Set/cleared by hardware each instruction cycle to indicate an odd/ even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in table 1, table 2, and table 3.

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB-C501. Table 3 illustrates the contents of the SFRs.

Table 1, Special Function Registers in numeric order of their addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**$0FF_H$**	**98_H**	**SCON** [1]	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H [2]
82_H	DPL	00_H	$9A_H$	reserved	XX_H [2]
83_H	DPH	00_H	$9B_H$	reserved	XX_H [2]
84_H	reserved	XX_H [2]	$9C_H$	reserved	XX_H [2]
85_H	reserved	XX_H [2]	$9D_H$	reserved	XX_H [2]
86_H	reserved	XX_H [2]	$9E_H$	reserved	XX_H [2]
87_H	PCON	0XXX0000B [2]	$9F_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**$0FF_H$**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H [2]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H [2]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H [2]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H [2]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	$A6_H$	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**$0FF_H$**	**$A8_H$**	**IE** [1]	**0X000000B** [2]
91_H	reserved	00_H	$A9_H$	reserved	XX_H [2]
92_H	reserved	XX_H [2]	AA_H	reserved	XX_H [2]
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved

Table 1, Special Function Registers in numeric order of their addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3**[1]	**$0FF_H$**	**$D8_H$**	reserved	XX_H[2]
$B1_H$	reserved	XX_H[2]	$D9_H$	reserved	XX_H[2]
$B2_H$	reserved	XX_H[2]	DA_H	reserved	XX_H[2]
$B3_H$	reserved	XX_H[2]	DB_H	reserved	XX_H[2]
$B4_H$	reserved	XX_H[2]	DC_H	reserved	XX_H[2]
$B5_H$	reserved	XX_H[2]	DD_H	reserved	XX_H[2]
$N6_H$	reserved	XX_H[2]	DE_H	reserved	XX_H[2]
$B7_H$	reserved	XX_H[2]	DF_H	reserved	XX_H[2]
$B8_H$	**IP** [1]	**X0000000B** [2]	**$E0_H$**	**ACC** [1]	**00_H**
$B9_H$	reserved	XX_H[2]	$E1_H$	reserved	XX_H[2]
BA_H	reserved	XX_H[2]	$E2_H$	reserved	XX_H[2]
BB_H	reserved	XX_H[2]	$E3_H$	reserved	XX_H[2]
BC_H	reserved	XX_H[2]	$E4_H$	reserved	XX_H[2]
BD_H	reserved	XX_H[2]	$E5_H$	reserved	XX_H[2]
BE_H	reserved	XX_H[2]	$E6_H$	reserved	XX_H[2]
BF_H	reserved	XX_H[2]	$E7_H$	reserved	XX_H[2]
$C0_H$	reserved	XX_H[2]	**$E8_H$**	reserved	XX_H[2]
$C1_H$	reserved	XX_H[2]	$E9_H$	reserved	XX_H[2]
$C2_H$	reserved	XX_H[2]	EA_H	reserved	XX_H[2]
$C3_H$	reserved	XX_H[2]	EB_H	reserved	XX_H[2]
$C4_H$	reserved	XX_H[2]	EC_H	reserved	XX_H[2]
$C5_H$	reserved	XX_H[2]	ED_H	reserved	XX_H[2]
$C6_H$	reserved	XX_H[2]	EE_H	reserved	XX_H[2]
$C7_H$	reserved	XX_H[2]	EF_H	reserved	XX_H[2]
$C8_H$	**T2CON**	**00_H**	**$F0_H$**	**B** [1]	**00_H**
$C9_H$	T2MOD	XXXXXXX0B [2]	$F1_H$	reserved	XX_H[2]
CA_H	RC2L	00_H	$F2_H$	reserved	XX_H[2]
CB_H	RC2H	00_H	$F3_H$	reserved	XX_H[2]
CC_H	TL2	00_H	$F4_H$	reserved	XX_H[2]
CD_H	TH2	00_H	$F5_H$	reserved	XX_H[2]
CE_H	reserved	XX_H[2]	$F6_H$	reserved	XX_H[2]
CF_H	reserved	XX_H[2]	$F7_H$	reserved	XX_H[2]
$D0_H$	**PSW** [1]	**00_H**	**$F8_H$**	reserved	XX_H[2]
$D1_H$	reserved	XX_H[2]	$F9_H$	reserved	XX_H[2]
$D2_H$	reserved	XX_H[2]	FA_H	reserved	XX_H[2]
$D3_H$	reserved	XX_H[2]	FB_H	reserved	XX_H[2]
$D4_H$	reserved	XX_H[2]	FC_H	reserved	XX_H[2]
$D5_H$	reserved	XX_H[2]	FD_H	reserved	XX_H[2]
$D6_H$	reserved	XX_H[2]	FE_H	reserved	XX_H[2]
$D7_H$	reserved	XX_H[2]	FF_H	reserved	XX_H[2]

[1]: Bit-addressable Special Function Regist
[2]: X means that the value is indeterminate and the location is reserved

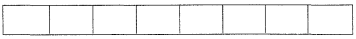
Table 2, Special Function Registers - Functional blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07H
Interrupt System	IE	Interrupt Enable Register	**$A8_H$** [1]	0X000000B [2]
	IP	Interrupt Priority Register	**$B8_H$** [1]	XX000000B [2]
Ports	P0	Port 0	**80_H** [1]	$0FF_H$
	P1	Port 1	**90_H** [1]	$0XX_H$ [3]
	P2	Port 2	**$A0_H$** [1]	$0FF_H$
	P3	Port 3	**$B0_H$** [1]	$0FF_H$
Serial Channels	PCON [2]	Power Control Register	87_H	0XXX0000B [2]
	SBUF	Serial Channel Buffer Reg.	99_H	$0XX_H$ [3]
	SCON	Serial Channel 0 Control Reg.	**98H** [1]	00_H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8DH_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
	T2MOD	Timer 2 Mode Register	$0C9_H$	00_H
	RC2H	Timer 2 Reload Capture Reg., High Byte	$0CB_H$	00_H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
Pow.Sav.Modes	PCON	Power Control Register	87_H	0XXX0000B [2]

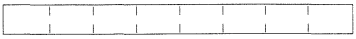
[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks
[3] X means that the value is indeterminate and the location is reserved

Table 3, Contents of SFRs, SFRs in numeric order

Address	Register	Bit 7	6	5	4	3	2	1	0
80_H	P0								
81_H	SP								
82_H	DPL								
83_H	DPH								
87_H	PCON	SMOD	–	–	–	GF1	GF0	PDE	IDLE
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0								
$8B_H$	TL1								
$8C_H$	TH0								
$8D_H$	TH1								
90_H	P1								
98_H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF								
$A0_H$	P2								
$A8_H$	IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$B0_H$	P3								
$B8_H$	IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
$C8_H$	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	–	–	–	–	–	–	–	DCEN



SFR bit and byte addressable



SFR not bit addressable

– : = this bit location is reserved

Table 3, Contents of SFRs, SFRs in numeric order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
CA_H	RC2L								
CB_H	RC2H								
CC_H	TL2								
CD_H	TH2								
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$	ACC								
$F0_H$	B								

SFR bit and byte addressable

SFR not bit addressable

– : = this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in table 4:

Table 4, Timer/Counter 0 and 1 operating modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/12 \times 32$	$f_{OSC}/24 \times 32$
1	16-bit timer/counter	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{OSC}/12$	$f_{OSC}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$

In the "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. Figure 2 illustrates the input clock logic.

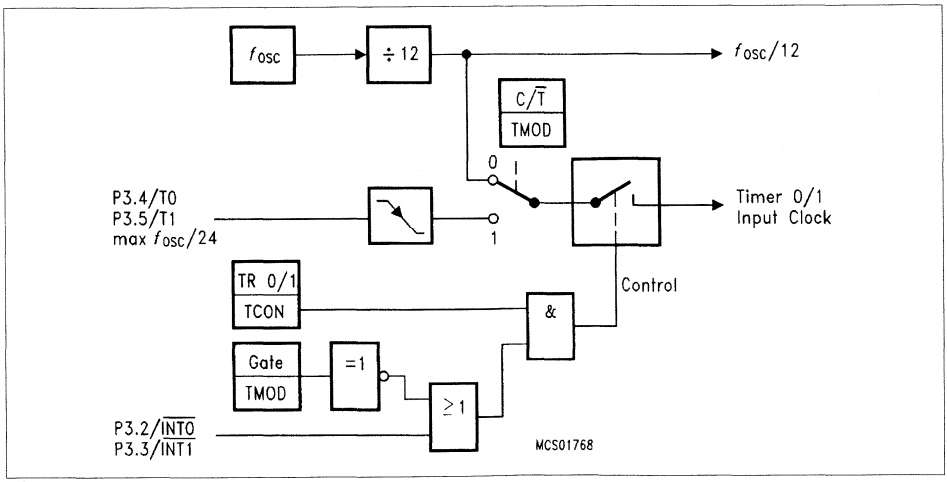


Figure 2, Timer/Counter 0 and 1 input clock logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5, Timer/Counter 2 operating modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ $\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting) capture TH2, TL2 → RC2H, RC2L	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓			
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2) extra external interrupt ("Timer 2")	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in table 6. The possible baudrates can be calculated using the formulas given in table 7.

Table 6, USART operating modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7, Formulas for calculating Baudrates

Baud rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate$) /32$ $(2^{SMOD} \times f_{OSC}) / (32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	f_{OSC} / (32 × (65536-(RC2H, RC2L))

Interrupt System

The SAB-C501 provides 6 interrupt sources with two priority levels. Figure 3 gives a general overview of the interrupt sources and illustrates the request and control flags.

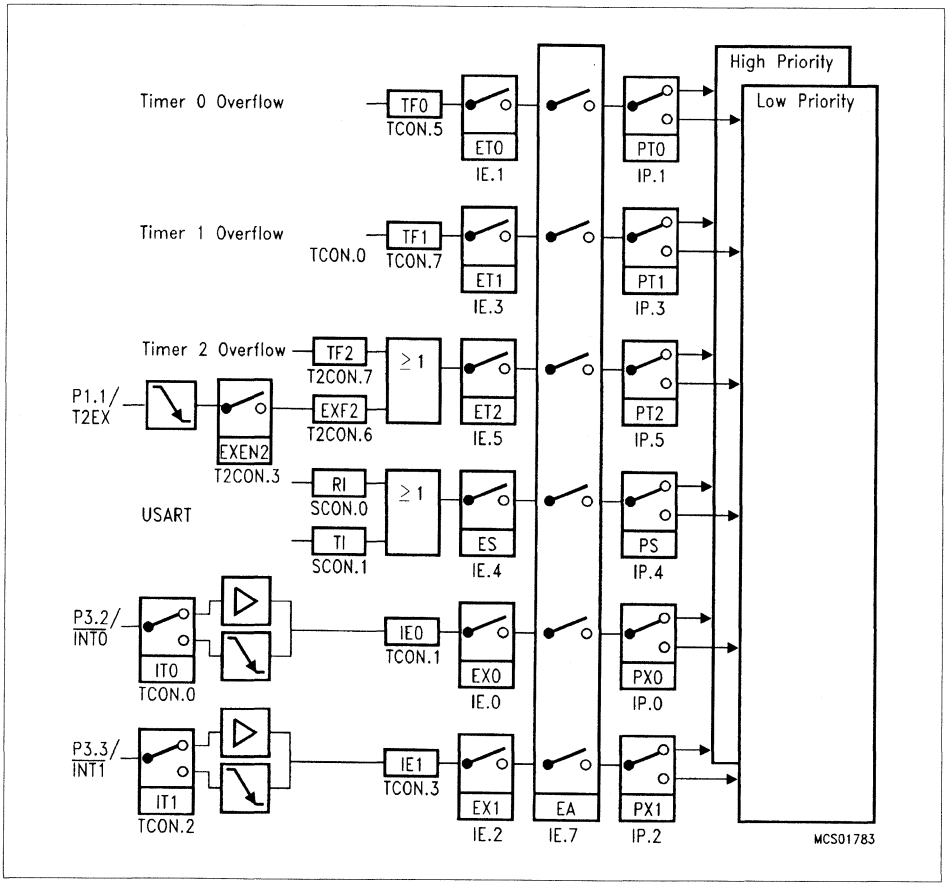


Figure 3, Interrupt Request Sources

Table 8, Interrupt sources and their corresponding interrupt vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in table 9.

Table 9, Interrupt priority-within-level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI + TI	
Timer 2 Interrupt,	TF2 + EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. Table 10 gives a general overview of the power saving modes.

Table 10, Power Saving modes overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (simulator to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... – 40 to + 85 °C
Storage temperature (T_{ST}) ..... – 65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition ..... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation ..... TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 20 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 20 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	TBD	µA	V_{CC} = 2 ... 5.5 V, [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; V_{AGND} = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

7) $I_{CC\,Max}$ at other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

AC Characteristics for SAB-C501-LN / C501-RN

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	60	–	$t_{CLCL} - 23$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C501 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L / C501-1R

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C501-L20 / C501-1R20

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
ALE low to valid instr in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-10	–	-10	–	ns

*) Interfacing the SAB-C501 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L20 / C501-1R20

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	20	–	$t_{CLCL} - 30$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	76	–	$2t_{CLCL} - 24$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C501-L40 / C501-1R40

Advance Information

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	2 t_{CLCL}-15	–	ns
Address setup to ALE	t_{AVLL}	10	–	t_{CLCL}-15	–	ns
Address hold after ALE	t_{LLAX}	10	–	t_{CLCL}-15	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	4 t_{CLCL}-45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	t_{CLCL}-15	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	–	3 t_{CLCL}-15	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	25	–	3 t_{CLCL}-50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	15	–	t_{CLCL}-10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	20	–	t_{CLCL}-5	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	5 t_{CLCL}-60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the SAB-C501 to devices with float times up to TBD ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L40 / C501-1R40 (cont'd)

Advance Information

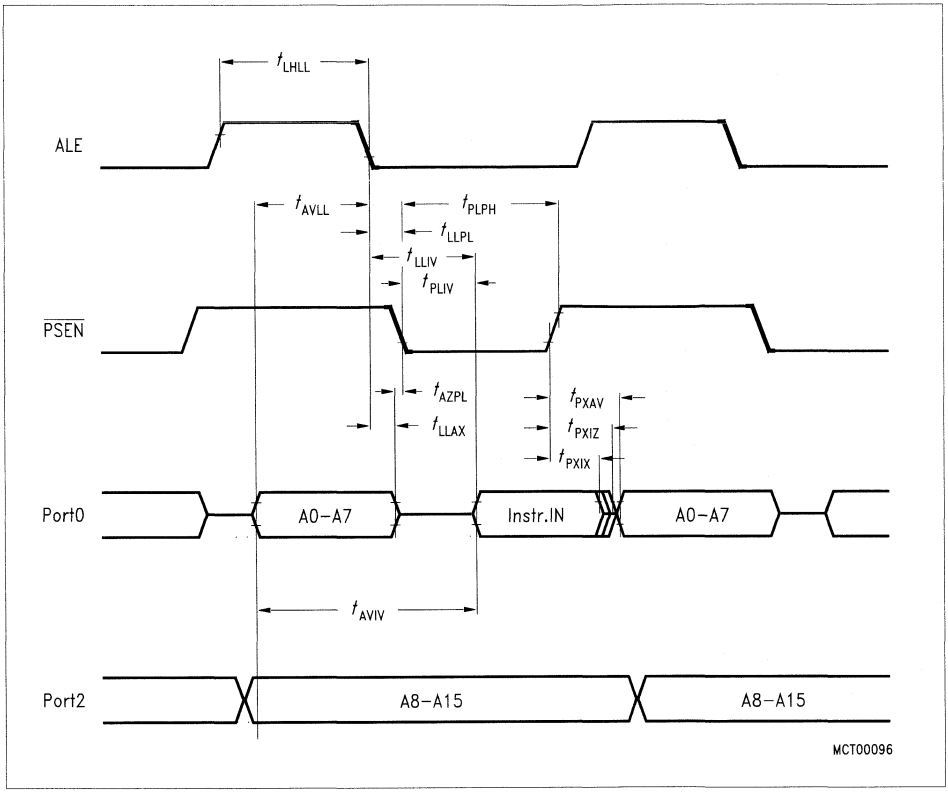
External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	6 t_{CLCL}-30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	6 t_{CLCL}-30	–	ns
Address hold after ALE	t_{LLAX2}	10	–	t_{CLCL}-15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5 t_{CLCL}-50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	2 t_{CLCL}+12	ns
ALE to valid data in	t_{LLDV}	–	150	–	8 t_{CLCL}-50	ns
Address to valid data in	t_{AVDV}	–	150	–	9 t_{CLCL}-75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3 t_{CLCL}-15	3 t_{CLCL}+15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	4 t_{CLCL}-30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL}-15	t_{CLCL}+15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL}-20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7 t_{CLCL}-50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	t_{CLCL}-20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

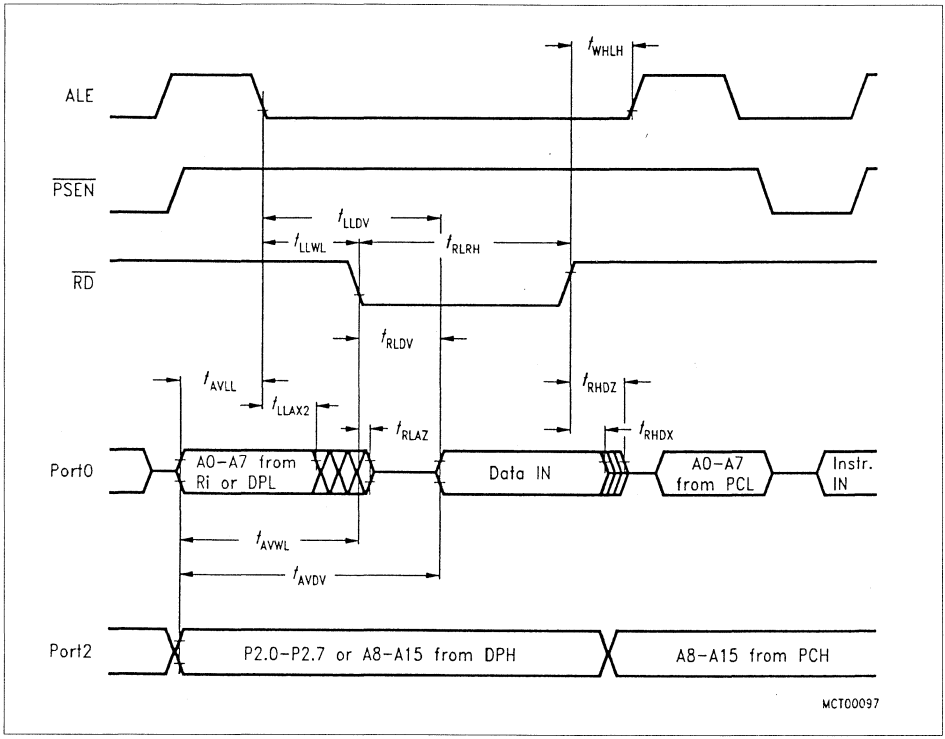
Advance Information

External Clock Drive

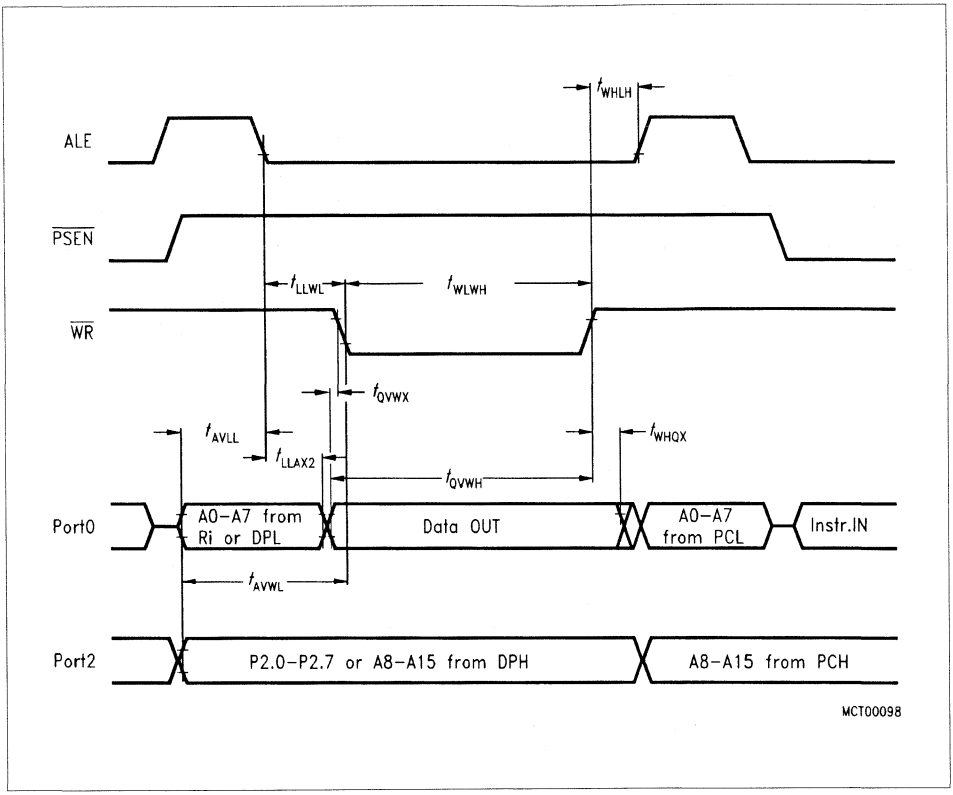
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	TBD	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	TBD	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	TBD	ns
Fall time	t_{CHCL}	–	TBD	ns



Program Memory Read Cycle



Data Memory Read Cycle

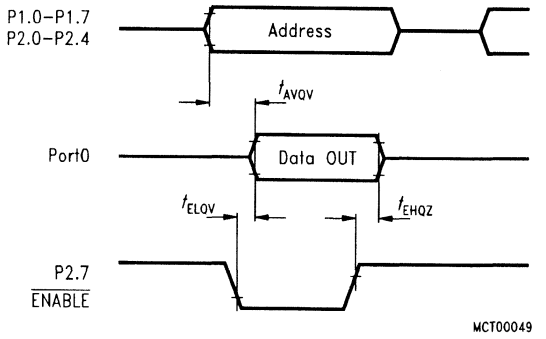


Data Memory Write Cycle

ROM Verification Characteristics for SAB-C501-1R

ROM Verification Mode 1

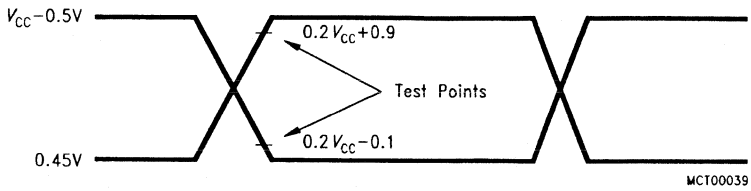
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

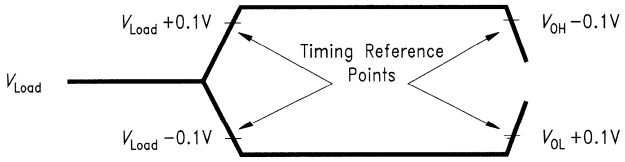
Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

ROM Verification Mode 1



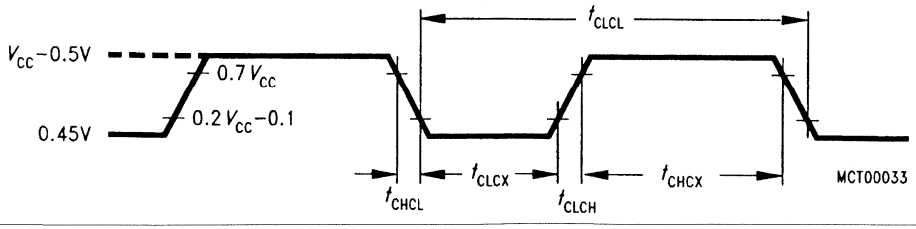
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms

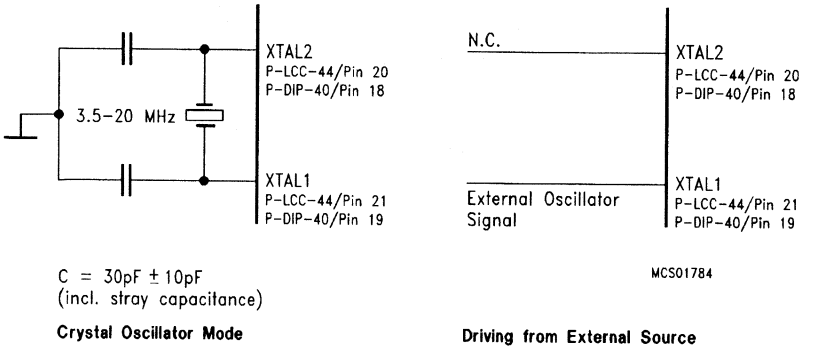


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs. I_{OL} / $I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



External Clock Cycle



Recommended Oscillator Circuits

SIEMENS

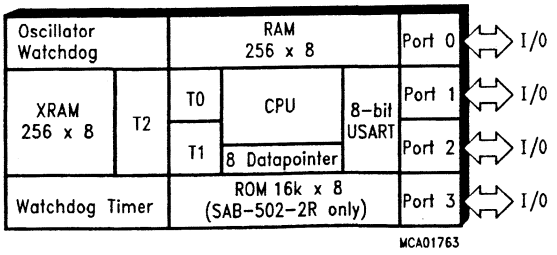
8-Bit CMOS Microcontroller

SAB-C502

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12 / 20 MHz operating frequency
- 16 K × 8 ROM (SAB-C502-2R only)
- 256 × 8 RAM
- 256 × 8 XRAM (additional on-chip RAM)
- Eight datapointers for indirect addressing of program and external data memory (including XRAM)
- Four 8-bit ports
- Three 16 -bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART with programmable 10-bit Baudrate-Generator
- Six interrupt sources, two priority levels
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- P-DIP-40 package and P-LCC-44 package
- Temperature ranges: SAB-C502 T_A: 0 °C to 70 °C
  SAF-C502 T_A: – 40 °C to 85 °C

SAB-C502



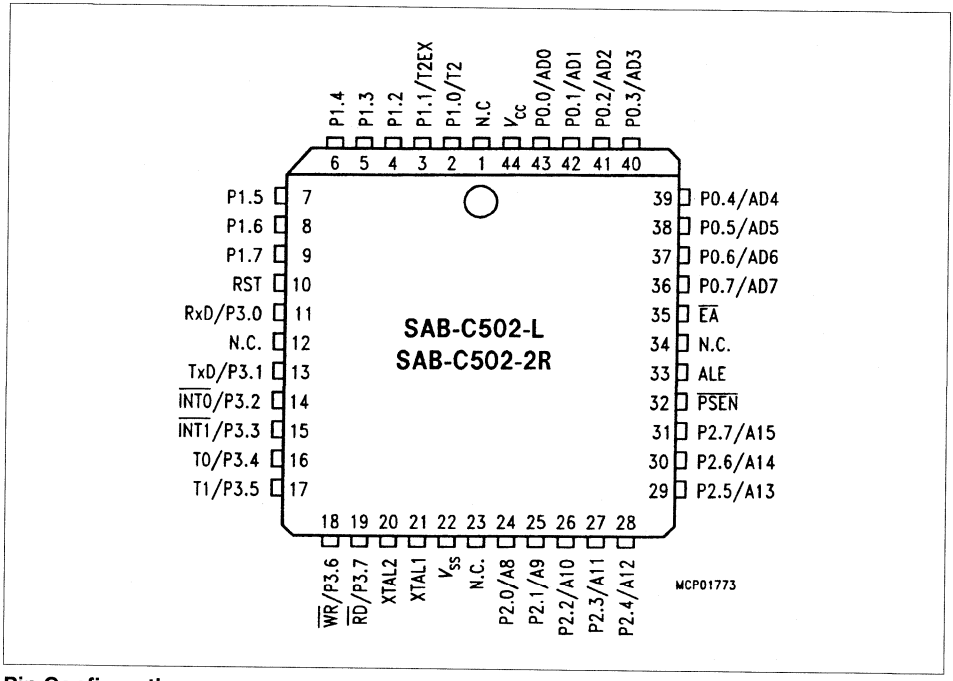
The SAB-C502-L/C502-2R described in this document is compatible with the SAB 80C52 and can be used for all present SAB 80C52 applications.

The SAB-C502-2R contains a non-volatile 16 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers/counters, a six source, two priority level interrupt structure, a serial port and versatile fail save mechanisms. The SAB-C502-L/C502-2R incorporates 256 × 8 additional on-chip RAM called XRAM. For higher performance eight datapointers are implemented. The SAB-C502-L is identical, except that it lacks the program memory on chip. Therefore the term SAB-C502 refers to both versions within this specification unless otherwise noted.

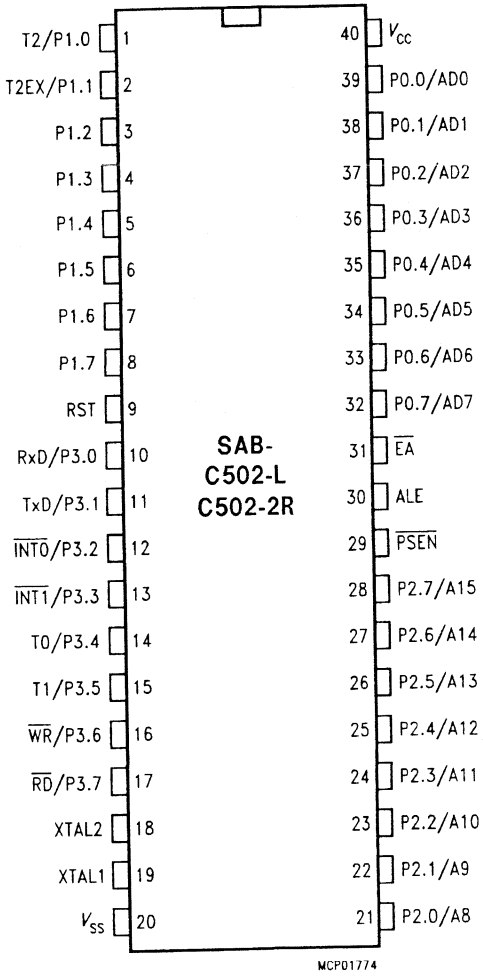
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C502-LN SAB-C502-LP	Q67120-C838 Q67120-C889	P-LCC-44 P-DIP-40	for external memory, 12 MHz
SAB-C502-2RN SAB-C502-2RP	Q67120-C839 Q67120-C890	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz
SAB-C502-L20N SAB-C502-L20P	Q67120-C885 Q67120-C891	P-LCC-44 P-DIP-40	for external memory 20 MHz
SAB-C502-2R20N SAB-C502-2R20P	Q67120-C884 Q67120-C892	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz
SAF-C502-LN SAF-C502-LP	Q67120-C883 Q67120-C893	P-LCC-44 P-DIP-40	for external ROM, 12 MHz, temp. – 40 °C to 85 °C
SAF-C502-2RN SAF-C502-2RP	Q67120-C886 Q67120-C894	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 °C to 85 °C
SAF-C502-L20N SAF-C502-L20P	Q67120-C887 Q67120-C895	P-LCC-44 P-DIP-40	for external memory, 20 MHz, temp. – 40 °C to 85 °C
SAF-C502-2R20N SAF-C502-2R20P	Q67120-C888 Q67120-C896	P-LCC-44 P-DIP-40	with factory mask-programmable ROM, 20 MHz, ext. temp. – 40 °C to 85 °C

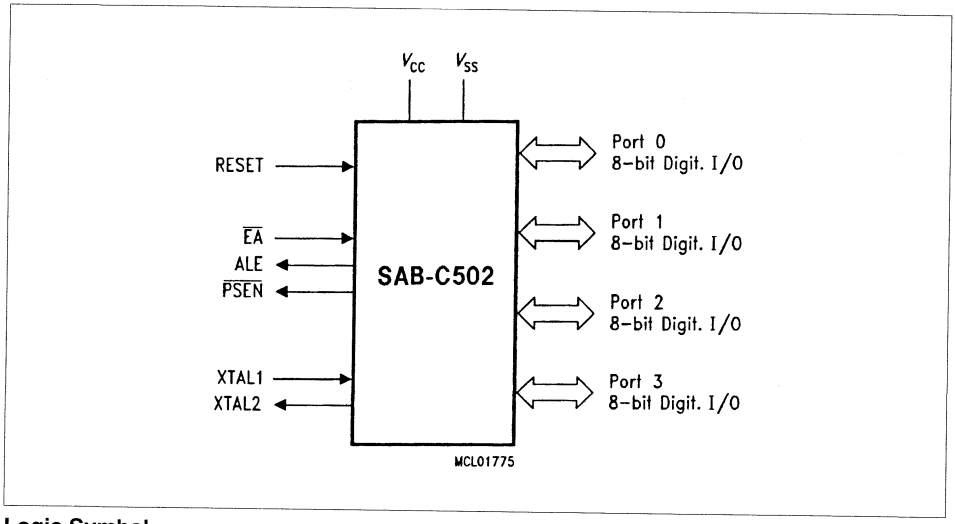
Note: extended temperature range – 40 °C to 110 °C (SAH-C502) on request.



Pin Configuration
(P-LCC-44)



Pin Configuration
(P-DIP-40)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P1.7 – P1.0	2–9	1–8	I	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate.
	2 3	1 2		The secondary functions are assigned to the pins of port 1, as follows: P1.0 T2 Input to counter 2 P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P3.0 – P3.7	11, 13–19	10–17	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10		P3.0 RxD receiver data input (asynchronous) or data input/output (synchronous) of serial interface 0
	13	11		P3.1 TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12		P3.2 $\overline{INT0}$ interrupt 0 $\overline{input}$/timer 0 gate control
	15	13		P3.3 $\overline{INT1}$ interrupt 1 $\overline{input}$/timer 1 gate control
	16	14		P3.4 T0 counter 0 input
	17	15		P3.5 T1 counter 1 input
	18	16		P3.6 $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17		P3.7 $\overline{RD}$ the read control signal enables the external data memory to port 0

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
XTAL1 XTAL2	21 20	19 18	– –	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL2** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	I/O	**Port 2** ia a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
RST	10	9	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE	33	30	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.
$\overline{EA}$	35	31	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB-C502-2R only) when the PC is less than 4000H. When held at low level, the SAB-C502 fetches all instructions from external program memory. For the SAB-C502-L this pin must be tied low.
P0.0 – P0.7	43–36	39–32	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB-C502-2R. External pull-up resistors are required during program verification.
V_{SS}	22	20	–	**Circuit ground potential**
V_{CC}	44	40	–	**Supply terminal** for all operating modes
N.C.	1, 12, 23, 24	–	–	**No connection**

*) I = Input
O = Output

Functional Description

The SAB-C502 is fully compatible to standard 8051 microcontroller.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52 the SAB-C502 incorporates some enhancements in the Timer2 and Fail Save Mechanism Unit.

Figure 1 shows a block diagram of the SAB-C502.

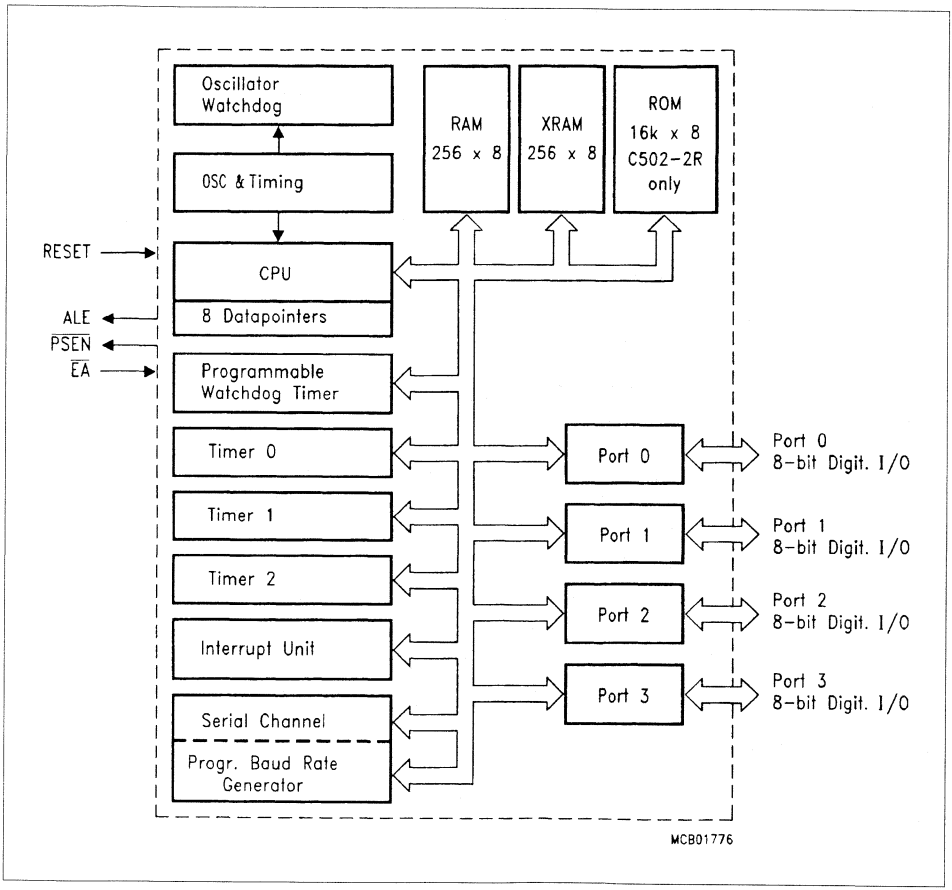


Figure 1: Block Diagram of the SAB-C502

CPU

The SAB-C502 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions execute in 1.0 µs (18 MHz : 667 ns).

Special Function Register PSW

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
Addr. 0D0H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxiliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address 00H - 07H
0	1	Bank 1 selected, data address 08H - 0FH
1	0	Bank 2 selected, data address 10H - 17H
1	1	Bank 3 selected, data address 18H - 1FH
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag.** Set/cleared by hardware each instruction cycle to indicate an odd/ even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 36 special function register (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in table 1, table 2 and table 3. In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB-C502. Table 3 illustrates the contents of the SFRs.

Table 1, Special Function Register in numeric order of their addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXH [2]
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	reserved		9CH	reserved	XXH [2]
85H	reserved		9DH	reserved	XXH [2]
86H	WDTREL	00H	9EH	reserved	XXH [2]
87H	PCON	000X0000B [2]	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IE** [1]	**0X000000B** [2]
91H	XPAGE	00H	A9H	reserved	XXH [2]
92H	DPSEL	XXXXX000B [2]	AAH	SRELL	0D9H
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	XCON	0F8H	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved

Table 1, Special Function Register in numeric order of their addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3** [1]	**0FFH**	**D8H**	**BAUD**	**0XXXXXXXB** [2]
B1H	SYSCON	XXXXXX01B [2]	D9H	reserved	XXH [2]
B2H	reserved	XXH [2]	DAH	reserved	XXH [2]
B3H	reserved	XXH [2]	DBH	reserved	XXH [2]
B4H	reserved	XXH [2]	DCH	reserved	XXH [2]
B5H	reserved	XXH [2]	DDH	reserved	XXH [2]
B6H	reserved	XXH [2]	DEH	reserved	XXH [2]
B7H	reserved	XXH [2]	DFH	reserved	XXH [2]
B8H	**IP** [1]	**XX000000B** [2]	**E0H**	**ACC** [1]	**00H**
B9H	reserved	XXH [2]	E1H	reserved	XXH [2]
BAH	SRELH	XXXXXX11B [2]	E2H	reserved	XXH [2]
BBH	reserved	XXH [2]	E3H	reserved	XXH [2]
BCH	reserved	XXH [2]	E4H	reserved	XXH [2]
BDH	reserved	XXH [2]	E5H	reserved	XXH [2]
BEH	reserved	XXH [2]	E6H	reserved	XXH [2]
BFH	reserved	XXH [2]	E7H	reserved	XXH [2]
C0H	**WDCON** [1]	**XXXX0000B** [2]	**E8H**	reserved	XXH [2]
C1H	reserved	XXH [2]	E9H	reserved	XXH [2]
C2H	reserved	XXH [2]	EAH	reserved	XXH [2]
C3H	reserved	XXH [2]	EBH	reserved	XXH [2]
C4H	reserved	XXH [2]	ECH	reserved	XXH [2]
C5H	reserved	XXH [2]	EDH	reserved	XXH [2]
C6H	reserved	XXH [2]	EEH	reserved	XXH [2]
C7H	reserved	XXH [2]	EFH	reserved	XXH [2]
C8H	**T2CON** [1]	**00H**	**F0H**	**B** [1]	**00H**
C9H	T2MOD	XXXXXXX0B [2]	F1H	reserved	XXH [2]
CAH	RC2L	00H	F2H	reserved	XXH [2]
CBH	RC2H	00H	F3H	reserved	XXH [2]
CCH	TL2	00H	F4H	reserved	XXH [2]
CDH	TH2	00H	F5H	reserved	XXH [2]
CEH	reserved	XXH [2]	F6H	reserved	XXH [2]
CFH	reserved	XXH [2]	F7H	reserved	XXH [2]
D0H	**PSW** [1]	**00H**	**F8H**	reserved	**XXH** [2]
D1H	reserved	XXH [2]	F9H	reserved	XXH [2]
D2H	reserved	XXH [2]	FAH	reserved	XXH [2]
D3H	reserved	XXH [2]	FBH	reserved	XXH [2]
D4H	reserved	XXH [2]	FCH	reserved	XXH [2]
D5H	reserved	XXH [2]	FDH	reserved	XXH [2]
D6H	reserved	XXH [2]	FEH	reserved	XXH [2]
D7H	reserved	XXH [2]	FFH	reserved	XXH [2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved

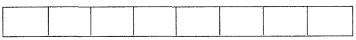
Table 2, Special Function Registers - Functional blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H**[1]	00H
	B	B-Register	**0F0H**[1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	DPSEL	Data pointer select register	92H	XXXX X000 B[3]
	PSW	Program Status Word Register	**0D0H**[1]	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	**0A8H**[1]	0X00 0000 B[3]
	IP	Interrupt Priority Register	**0B8H**[1]	XX00 0000 B[3]
Ports	P0	Port 0	**80H**[1]	0FFH
	P1	Port 1	**90H**[1]	0FFH
	P2	Port 2	**0A0H**[1]	0FFH
	P3	Port 3	**0B0H**[1]	0FFH
XRAM	XPAGE	Page addr. reg. for XRAM	91H	00H
	XCON	XRAM startaddress (highbyte)	94H	0F8H
	SYSCON	XRAM control register	0B1H	XXXX XX01B[3]
Serial Channels	PCON[2]	Power Control Register	87H	00H
	SBUF	Serial Channel Buffer Reg.	99H	0XXH[3]
	SCON	Serial Channel Control Reg.	**98H**[1]	00H
	SRELL	Baudrate Generator Reloadvalue, Lowbyte	AAH	0D9H
	SRELH	Baudrate Generator Reloadvalue, Highbyte	BAH	XXXX XX11B[3]
	BAUD	Baudrate Generator Enable Bit	**0D8H**[1]	0XXX XXXXB[3]
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88H**[1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	**0C8H**[1]	00H
	T2MOD	Timer 2 Mode Register	0C9H	XXXX XXX0 B[3]
	RC2L	Timer 2, Reload Capture Register, Low Byte	0CAH	00H
	RC2H	Timer 2, Reload Capture Register, High Byte	0CBH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
Watchdog	WDCON	Watchdog Timer Control Register	**0C0H**[1]	XXXX 0000B[3]
	WDTREL	Watchdog Timer Reload Reg.	86H	00H
Pow.Sav. Modes	PCON[2]	Power Control Register	87H	000X 0000B[3]

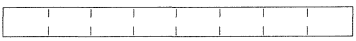
[1]: Bit-addressable special function registers
[2]: This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3]: X means that the value is indeterminate and the location is reserved

Table 3, Contents of SFR's, SFR's in numeric order

Address	Register	Bit 7	6	5	4	3	2	1	0
80H	P0								
81H	SP								
82H	DPL								
83H	DPH								
86H	WDTREL								
87H	PCON	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
8AH	TL0								
8BH	TL1								
8CH	TH0								
8DH	TH1								
90H	P1								
91H	XPAGE								
92H	DPSEL	–	–	–	–	–	.2	.1	.0
94H	XCON								
98H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99H	SBUF								
A0H	P2								
A8H	IE	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
AAH	SRELL								



bit and byte addressable



not bit addressable

– = reserved

Table 3, Contents of SFRs, SFRs in numeric order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
B0H	P3								
B1H	SYSCON	–	–	–	–	–	–	XMAP1	XMAP0
B8H	IP	–	PADC	PT2	PS	PT1	PX1	PT0	PX0
BAH	SRELH								
C0H	WDCON	–	–	–	–	OWDS	WDTS	WDT	SWDT
C8H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
C9H	T2MOD	–	–	–	–	–	–	–	DCEN
CAH	RC2L								
CBH	RC2H								
CCH	TL2								
CDH	TH2								
D0H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
D8H	BAUD	BD	–	–	–	–	–	–	–
E0H	ACC								
F0H	B								

bit and byte addressable

not bit addressable

– = reserved

Timer/Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in table 4:

Table 4, Timer/Counter 0 and 1 operating modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/_{12 \times 32}$	$f_{OSC}/_{24 \times 32}$
1	16-bit timer/counter	X	X	0	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$

In "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. Figure 2 illustrates the input clock logic.

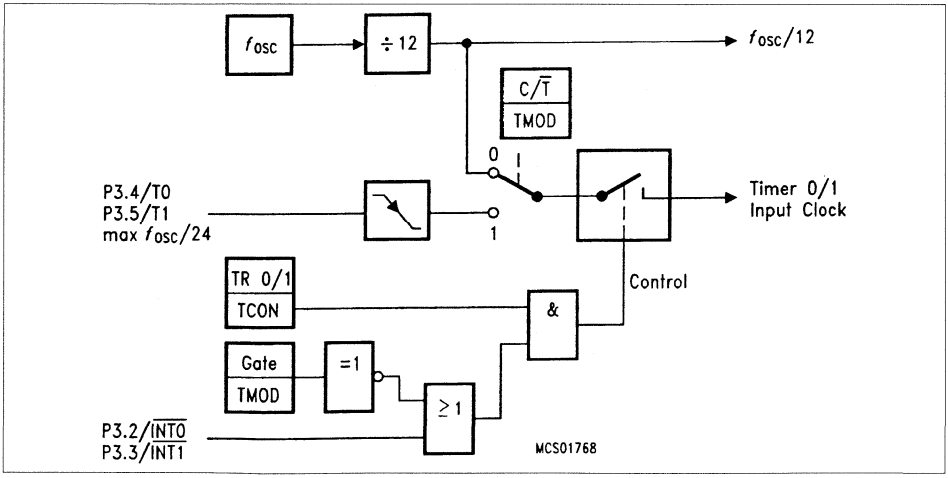


Figure 2, Timer/Counter 0 and 1 input clock logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5, Timer/Counter 2 operating modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ $\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{OSC}/12$	max $f_{OSC}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Cap-ture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting) capture TH2, TL2 → RC2H, RC2L	$f_{OSC}/12$	max $f_{OSC}/24$
	0	1	1	X	1	↓			
Baud Rate Gene-rator	1	X	1	X	0	X	no overflow interrupt request (TF2) extra external interrupt ("Timer 2")	$f_{OSC}/2$	max $f_{OSC}/24$
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in table 6. Figure 3 illustrates the block diagram of Baudrate generation for the serial interface.

Table 6, USART operating modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate or Baudrate Generator	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate or Baudrate Generator	9-bit UART Like mode 2 except the variable baud rate

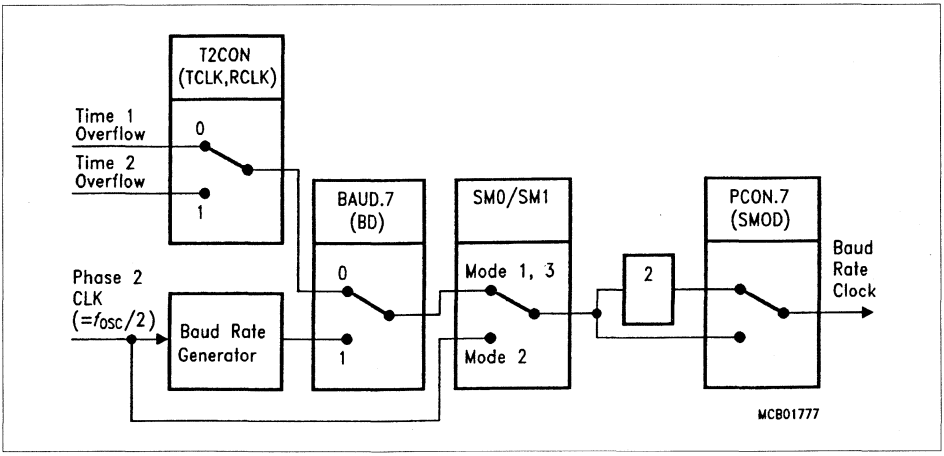


Figure 3, Block Diagram of Baud Rate Generation for Serial Interface

The possible baudrate can be calculated using the formulas given in table 7.

Table 7, Baudrates

Baud rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC})/64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	(2^{SMOD} × timer 1 overflow rate)/32 $(2^{SMOD} \times f_{OSC})/(32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	$f_{OSC}/(32 \times (65536\text{-(RC2H, RC2L)}))$
Baudrate Generator	1,3	$(2^{SMOD} \times f_{OSC})/(64 \times (2^{10}\text{-SREL}))$

The internal baudrate generator consists of a free running 10-bit timer with $f_{OSC}/2$ input frequency. The internal baudrate generator is selected by setting bit BD in SFR BAUD.

Additional On-Chip RAM - XRAM

The SAB-C502 contains another 256byte of On-Chip RAM additional to the 256bytes internal RAM. This RAM is called XRAM ('eXtended RAM') in this document.

The additional ON-Chip RAM is logically located in the external data memory range. The highbyte of the XRAM address range startaddress is programmable by SFR XCON (94H). The reset value of XCON is 0F8H (that is, XRAM address range F800H ... F8FFH).

The contents of the XRAM is not affected by a reset. After power up the contents is undefined, while it remains unchanged during and after reset as long as the power supply is not turned off. The XRAM is controlled by SFR SYSCON as shown in table 8.

Table 8, Control of the XRAM

SFR SYSCON		Description
XMAP1	XMAP0	
0	1	Resetvalue. Access to XRAM is disabled. When cleared it can be set again only by a reset
0	0	XRAM enabled
1	0	XRAM enabled. The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM

Because of the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM. A general overview gives table 9.

Table 9, Accessing the XRAM

Instruction using	Instruction	Remarks
DPTR	MOVX A @DPTR MOVX @ DPTR,A	Normally the use of these instructions would use a physically external memory. However, in the SAB-C502 the XRAM is accessed if it is enabled.
R0/R1 (page mode)	MOVX A, @Ri MOVX@Ri,A	Normally Port 2 serves as page register. However, the distinction, whether Port 2 is as general purpose I/O or as "page address" is made by the external design. Hence a special SFR XPAGE is implemented the serve the same function for the XRAM as Port 2 for external data memory.

Note: When writing the page address (in page mode) at Port2 the value is also written in XPAGE. However when writing XPAGE the value at PORT2 is not changed!

The behaviour of Port0/Port2 and $\overline{RD}$/$\overline{WR}$ during MOVX accesses is shown in table 10.

Table 10, Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR outside XRAM address range (DPH ≠ XCON)	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	DPTR within XRAM address range (DPH = XCON)	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
MOVX @Ri	XPAGE outside XRAM addr. page range (XPAGE ≠ XCON)	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	XPAGE within XRAM addr. page range (XPAGE = XCON)	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used

(shaded) modes compatible to the standard 8051-family

Eight Datapointers for Faster External Bus Access

The SAB-C502 contains a set of eight 16-bit-Datapointer (DPTR) from which the actual DPTR can be selected.

This means that the user's program may keep up to eight 16-bit addresses resident in these registers, but only one register at the time is selected to be the datapointer. Thus the DPTR in turn is accessed (or selected) via indirect addressing. This indirect addressing is done through a special function register (SFR) called DPSEL (data pointer select register, Bits 0 to 2). All instructions of the SAB-C502 which handle the DPTR therefore affect only one of the eight pointers which is addressed by DPSEL at that very moment.

A 3-bit field in SFR DPSEL points to the currently used DPTRx:

DPSEL			selected DPTR
.2	.1	.0	
0	0	0	DPTR 0
0	0	1	DPTR 1
0	1	0	DPTR 2
0	1	1	DPTR 3
1	0	0	DPTR 4
1	0	1	DPTR 5
1	1	0	DPTR 6
1	1	1	DPTR 7

Interrupt System

The SAB-C502 provides 6 interrupt sources with two priority levels. Figure 4 gives a general overview of the interrupt sources and illustrates the request and control flags.

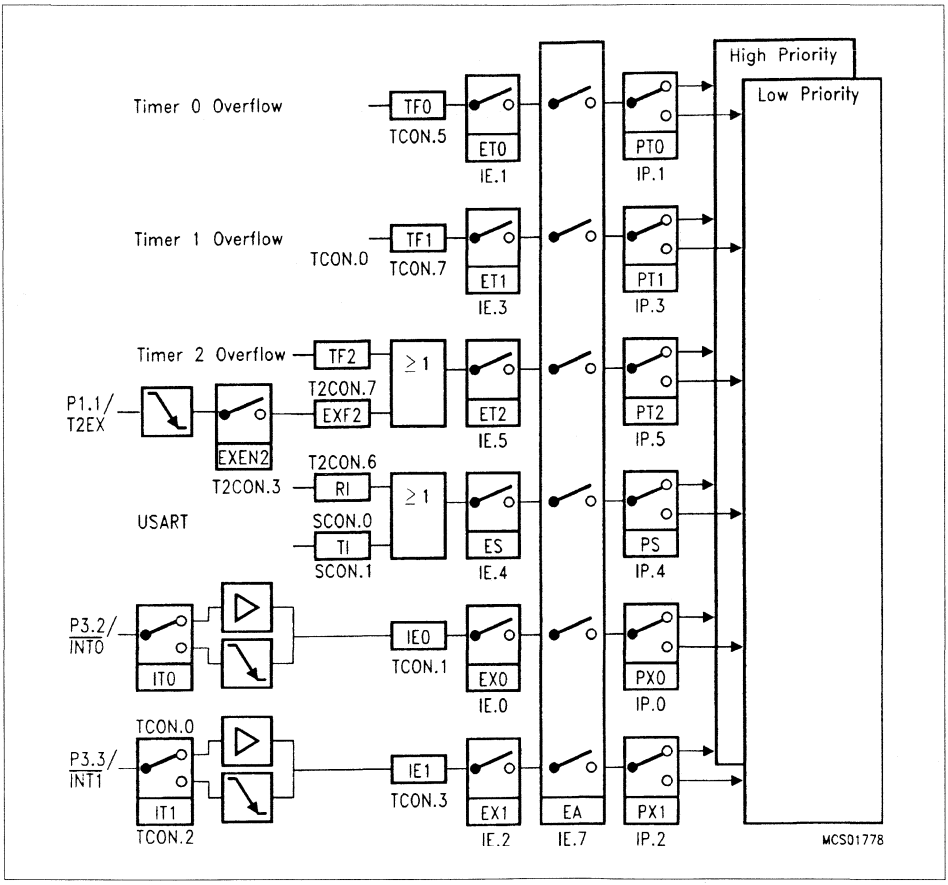


Figure 4, Interrupt Request Sources

Table 11, Interrupt sources and their corresponding interrupt vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in table 12.

Table 12, Interrupt priority-within-level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI or TI	
Timer 2 Interrupt,	TF2 or EXF2	Low

Fail Safe Mechanisms

The SAB-C502 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure.

1) Watchdog Timer (15 bit, WDT)

2) Oscillator Watchdog (OWD)

1) Watchdog Timer (WDT)

The Watchdog Timer in the SAB-C502 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler. The latter is enabled by setting bit WDTREL.7.

Figure 5 shows the block diagram of the programmable Watchdog Timer.

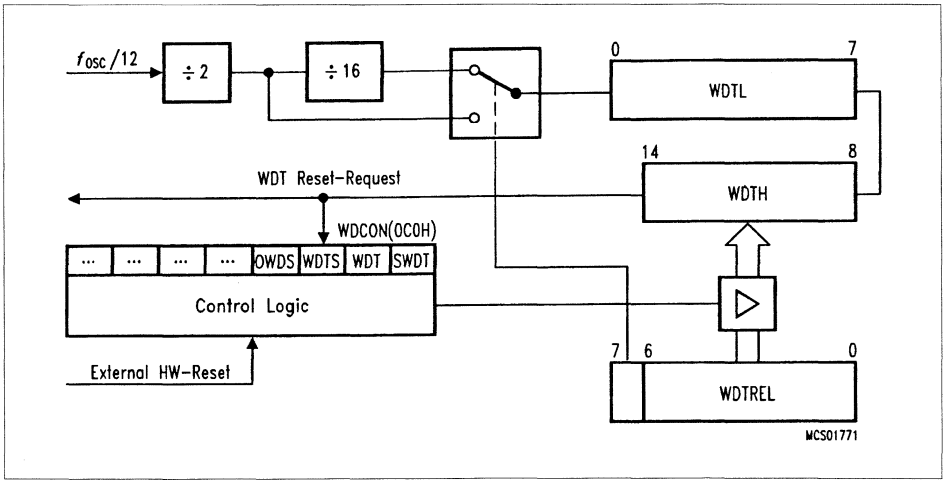


Figure 5, Block Diagram of the Programmable Watchdog Timer

– Starting and refreshing the WDT

Table 13 gives an overview how to start and refresh the WDT. The mentioned bits are located in SFR WDCON.

Table 13, Starting and refreshing the WDT

Function	Example		Remarks
Starting WD	SETB	SWDT	Cannot be stopped during active mode of the device. WDT is halted during idle mode, power down mode or the oscillator watchdog reset is active.
Refreshing WD	SETB SETB	WDT SWDT	Double instruction sequence (setting bit WDT and SWDT consecutively) to increase system security.

– Watchdog reset and watchdog status flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state 7FFCH. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS (SFR WDCON) is set. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

2) Oscillator Watchdog (OWD)

The OWD consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

Figure 6 shows the block diagram of the oscillator watchdog unit while table 14 shows the effect when the OWD becomes activ/inactiv.

Note: The OWD is always enabled!

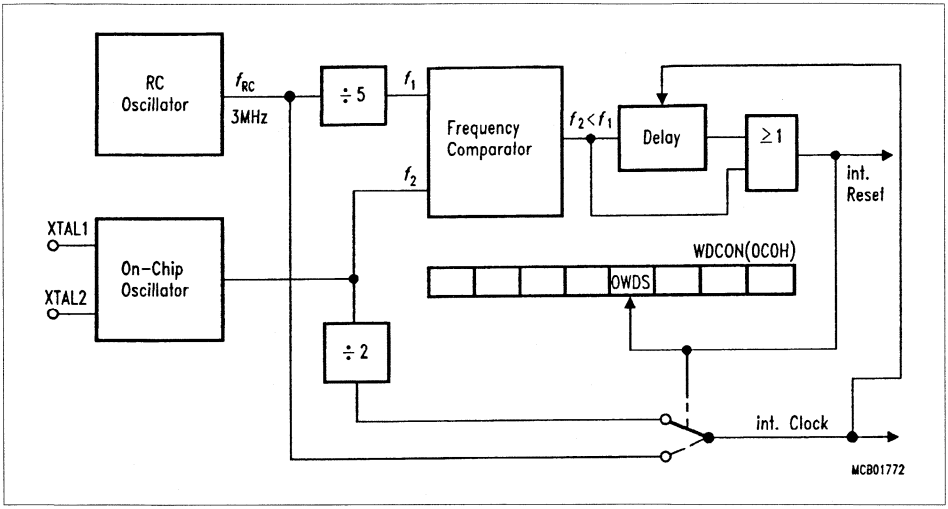


Figure 6, Functional Block Diagram of the Oscillator Watchdog

Table 14, Effects of the OWD

Conditions	Effect
$f_{OSC} < f_{RC}/5$	Switch input of internal clock system to RC oscillator output Activating internal reset at the same time (reset sequence is clocked by RC-oscillator). Exception from effects of a Hardware Reset: Watchdog Timer Status Flag, WDTS is not reset Oscillator Watchdog Status Flag, OWDS is set
$f_{OSC} > f_{RC}/5$	Input of internal clock system is $f_{OSC}/2$. When failure condition ($f_{OSC} < f_{RC}/5$) disappears the part executes a final reset phase of typ. 1 ms in order to allow the external oscillator to stabilize.

Power Saving Modes

Two power down modes are available, the Idle Mode and the Power Down Mode.

The bits PDE, PDS and IDLE, IDLS select the Power Down mode or the idle mode, respectively. If the Power Down mode and the idle mode are set at the same time, Power Down takes precedence. Table 15 gives a general overview of the power saving modes.

Table 15, Entering and leaving the power saving modes

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active Double instruction sequence
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillators are stopped. Contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR's contents.) Double instruction sequence

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... – 40 °C to + 85 °C
Storage temperature (T_{ST}) ..... – 65 °C to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition ..... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation ..... TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 to + 70 °C for the SAB-C502
T_A = – 40 to + 85 °C for the SAF-C502

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{EA}$, RESET, XTAL1)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to RESET, $\overline{EA}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA[1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA[1]
Output high voltage (ports 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA[2], I_{OH} = – 80 µA[2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, P1)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz[7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz[7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V,[5]
Active mode, 20 MHz[7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V,[4]
Idle mode, 20 MHz[7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V,[5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V,[3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = RESET = Port0 = V_{CC}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

7) $I_{CC\,Max}$ at other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

AC Characteristics for SAB-C502-L / C502-2R

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to + 70 °C for the SAB-C502
T_A = – 40 °C to + 85 °C for the SAF-C502

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	60	–	$t_{CLCL} - 23$	–	ns
Address to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C502-L/C502-2R to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C502-L / C502-2R

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C502-L20 / C502-2R20

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to + 70 °C for the SAB-C502
T_A = – 40 °C to + 85 °C for the SAF-C502

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
Address to valid instr in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C502-L20/C502-2R20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

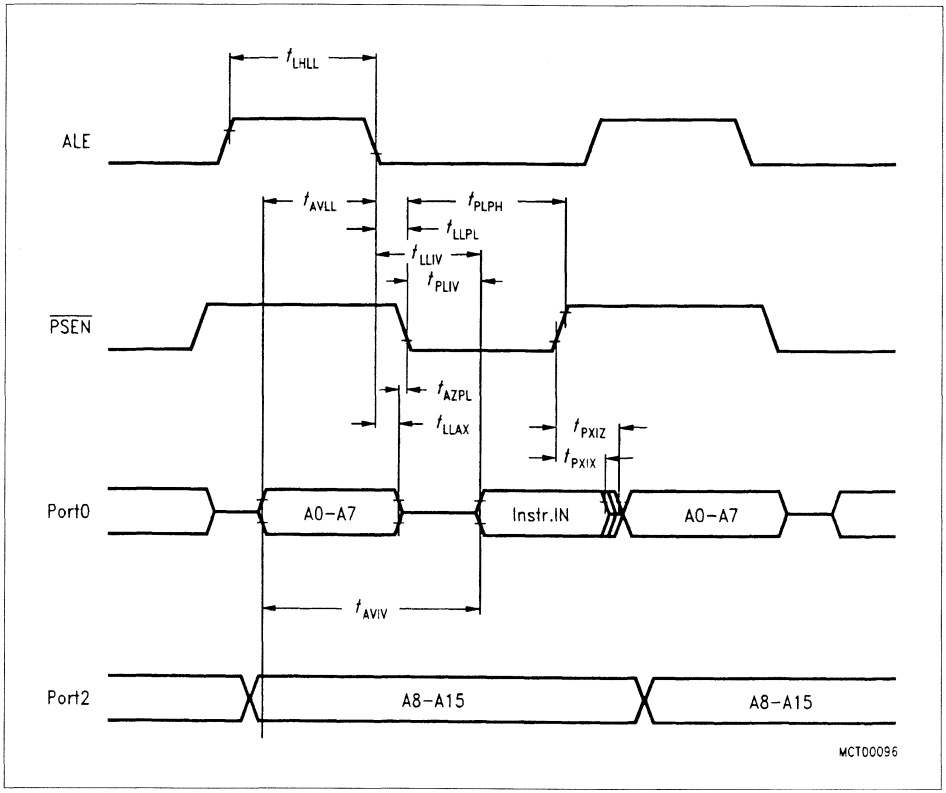
AC Characteristics for SAB-C502-L20 / C502-2R20

External Data Memory Characteristics

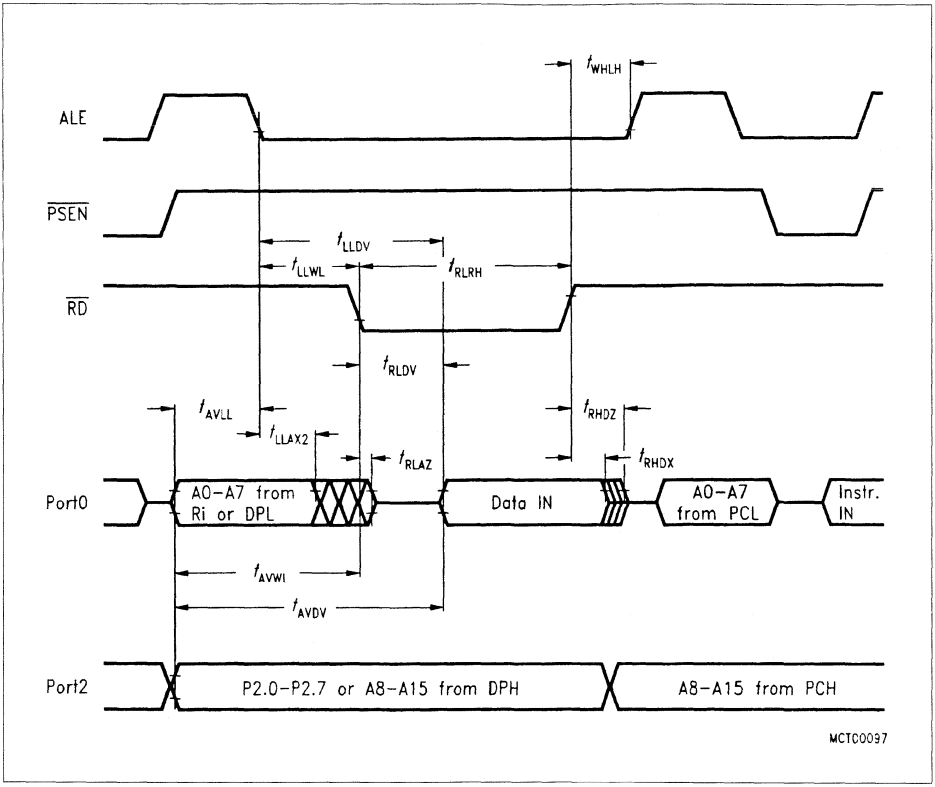
Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	65	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	40	–	$2t_{CLCL} - 60$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

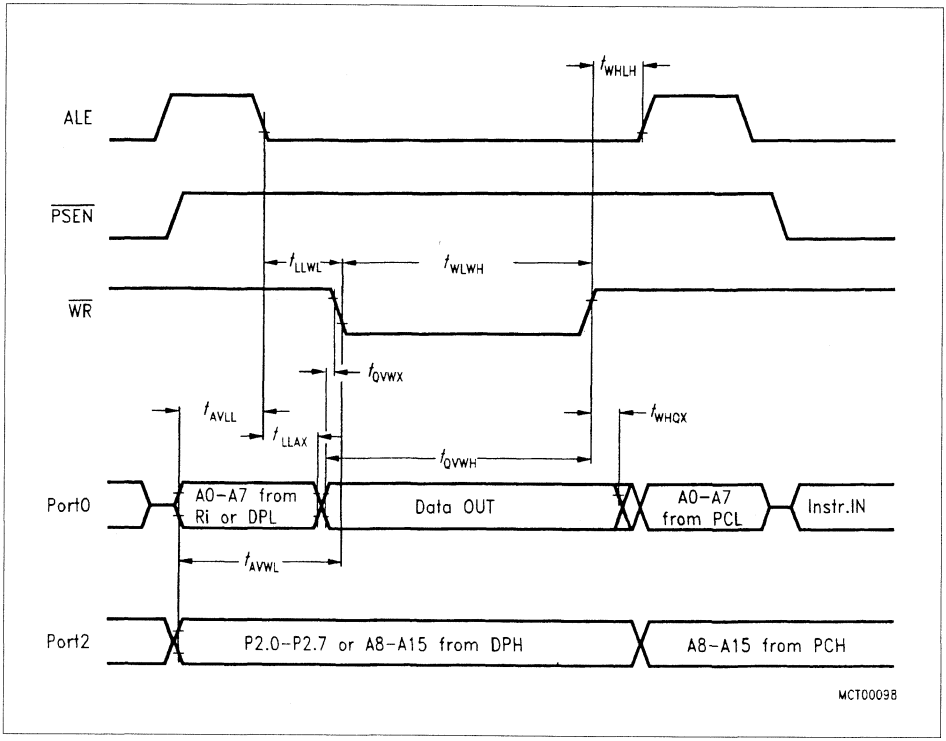
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



Program Memory Read Cycle



Data Memory Read Cycle

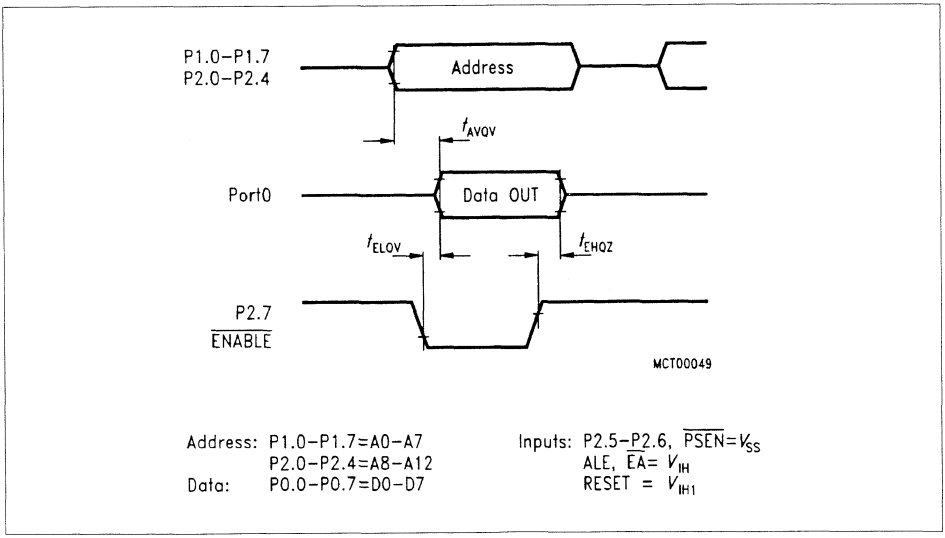


Data Memory Write Cycle

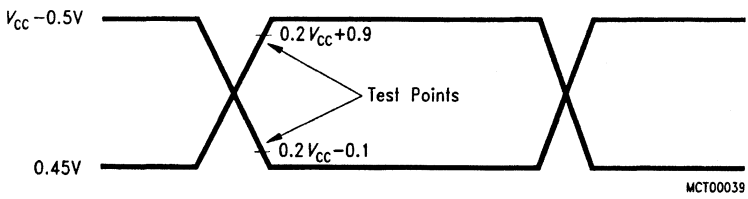
ROM Verification Characteristics for SAB-C502-2R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

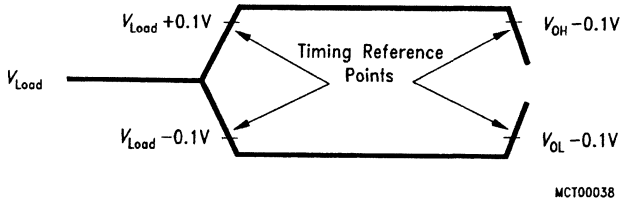


ROM Verification Mode 1



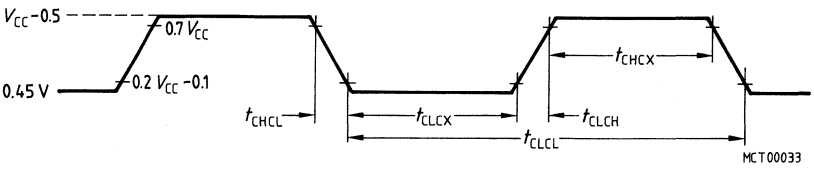
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms

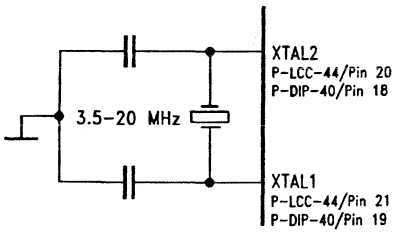


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs. I_{OL} / I_{OH} ≥ ± 20 mA.

AC Testing: Float Waveforms

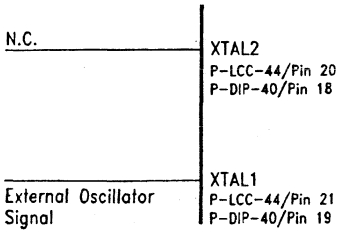


External Clock Cycle



C = 30pF ± 10pF
(incl. stray capacitance)

Crystal Oscillator Mode



MCS01784

Driving from External Source

Recommended Oscillator Circuits

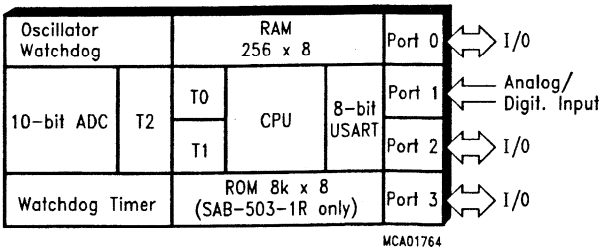
SIEMENS

8-Bit CMOS Microcontroller — SAB-C503

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12 / 20 MHz operating frequency
- 8 K × 8 ROM (SAB-C503-1R only)
- 256 × 8 RAM
- Four 8-bit ports, (including one input port for digital or analog input)
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Genuine 10-bit A/D Converter with 8 multiplexed inputs
- Seven interrupt sources, two priority levels
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- P-LCC-44 package
- Temperature ranges: SAB-C503 T_A: 0 °C to 70 °C
  SAF-C503 T_A: – 40 °C to 85 °C

SAB-C503



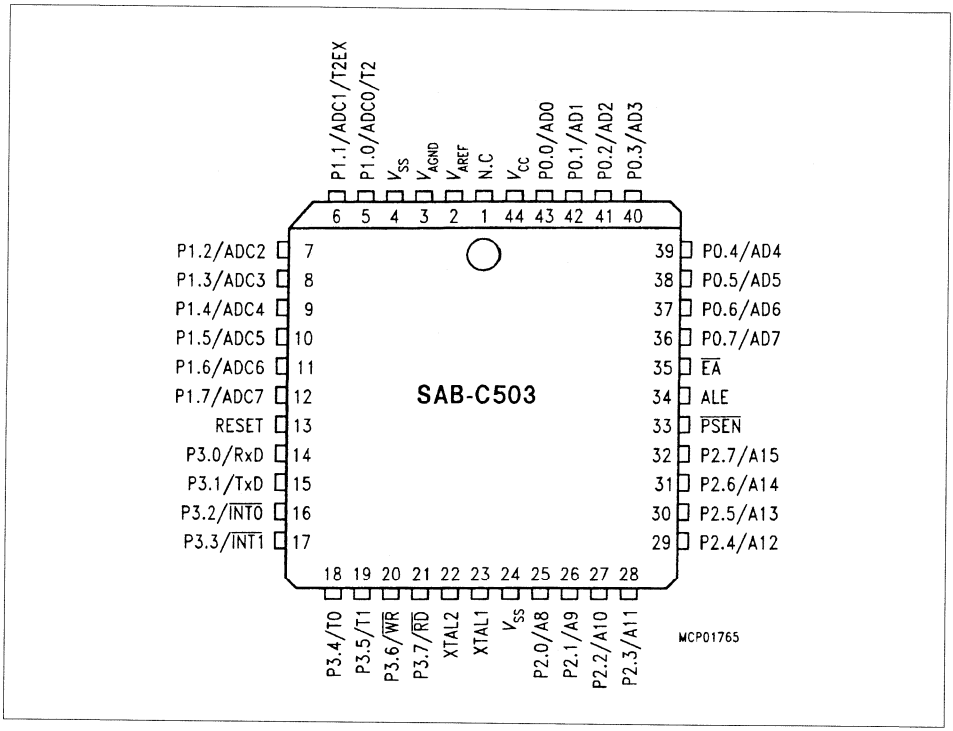
The SAB-C503-L/C503-1R described in this document is compatible (not pin-compatible) with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

The SAB-C503-1R contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers/counters, a seven source, two priority level interrupt structure, a serial port, versatile fail save mechanisms and a genuine 10-bit A/D Converter. The SAB-C503-L is identical, except that it lacks the program memory on chip. Therefore the term SAB-C503 refers to both versions within this specification unless otherwise noted.

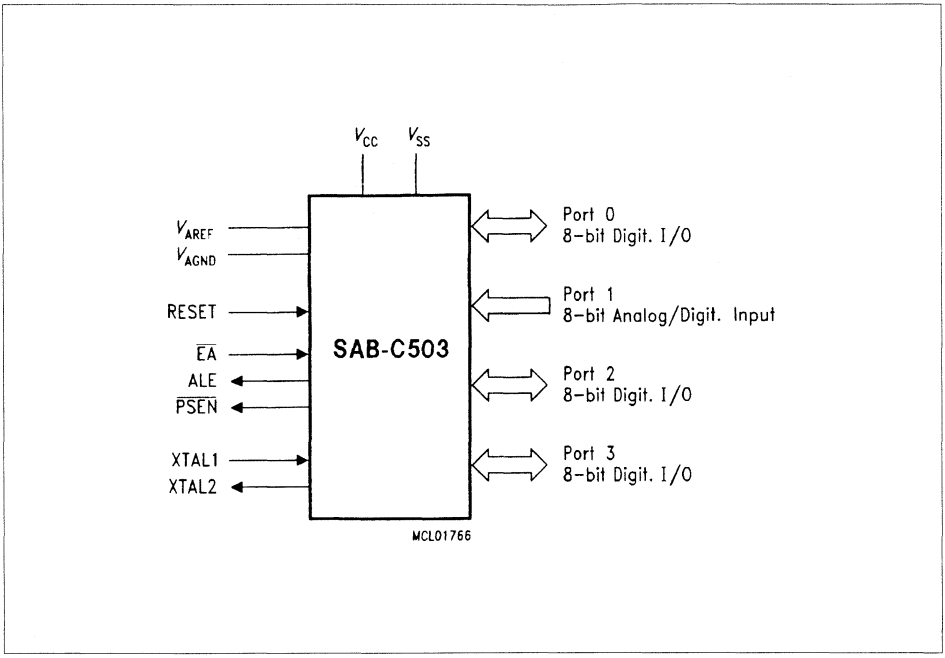
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C503-LN	Q67120-C835	P-LCC-44	for external memory, 12 MHz
SAB-C503-1RN	Q67120-C834	P-LCC-44	with factory mask-programmable ROM, 12 MHz
SAB-C503-L20N	Q67120-C877	P-LCC-44	for external memory, 20 MHz
SAB-C503-1R20N	Q67120-C878	P-LCC-44	with factory mask-programmable ROM, 20 MHz
SAF-C503-LN	Q67120-C879	P-LCC-44	for external ROM, 12 MHz, ext. temp. – 40 °C to 85 °C
SAF-C503-1RN	Q67120-C880	P-LCC-44	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 °C to 85 °C
SAF-C503-L20N	Q67120-C881	P-LCC-44	for external memory, 20 MHz, ext. temp. – 40 °C to 85 °C
SAF-C503-1R20N	Q67120-C882	P-LCC-44	with factory mask-programmable ROM, 20 MHz, ext. temp. – 40 °C to 85 °C

Note: extended temperature range – 40 °C to 110 °C (SAH-C503) on request.



Pin Configuration
(P-LCC-44)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number P-LCC-44	I/O *)	Function
P1.7 – P1.0	12–5	I	**Port 1** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high low voltages, and for the multiplexed analog inputs of the A/D-Converter, simultaneously. Port 1 also contains the timer 2 pins as secondary function. The secondary functions are assigned to the pins of port 1, as follows:
	5		P1.0 AN0 / T2 Analog input channel 0 Input to counter 2
	6		P1.1 AN1 / T2EX Analog input channel 1 Capture - Reload trigger of timer 2 / Up-Down count
	7		P1.2 AN2 Analog input channel 2
	8		P1.3 AN3 Analog input channel 3
	9		P1.4 AN4 Analog input channel 4
	10		P1.5 AN5 Analog input channel 5
	11		P1.6 AN6 Analog input channel 6
	12		P1.7 AN7 Analog input channel 7

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-LCC-44	I/O *)	Function
P3.0 – P3.7	14–21	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: 14 – RxD (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface 15 – TxD (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control 16 – $\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control 17 – T0 (P3.4): counter 0 input 18 – T1 (P3.5): counter 1 input 19 – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory 20 – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0 21

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-LCC-44	I/O *)	Function
XTAL2	22	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	23	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times a well as rise/fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	25–32	I/O	**Port 2** ia a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	33	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
RESET	13	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-LCC-44	I/O *)	Function
ALE	34	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.
$\overline{EA}$	35	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB-C503-1R only) when the PC is less than 2000H. When held at low level, the SAB-C503 fetches all instructions from external program memory. For the SAB-C503-L this pin must be tied low.
P0.0 – P0.7	43–36	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB-C503-1R. External pull-up resistors are required during program verification.
V_{AREF}	2		**Reference voltage** for the A/D converter.
V_{AGND}	3		**Reference ground** for the A/D converter.
V_{SS}	4, 24	–	**Circuit ground potential**
V_{CC}	44	–	**Supply terminal** for all operating modes
N.C.	1	–	**No connection**

*) I = Input
O = Output

Functional Description

The SAB-C503 is fully compatible to standard 8051 microcontroller.

It is compatible with the SAB 80C52 but not pin-compatible. While maintaining all architectural and operational characteristics of the SAB 80C52 the SAB-C503 incorporates a genuine 10-bit A/D Converter as well as some enhancements in the Timer2 and Fail Save Mechanism Unit.

Figure 1 shows a block diagram of the SAB-C503.

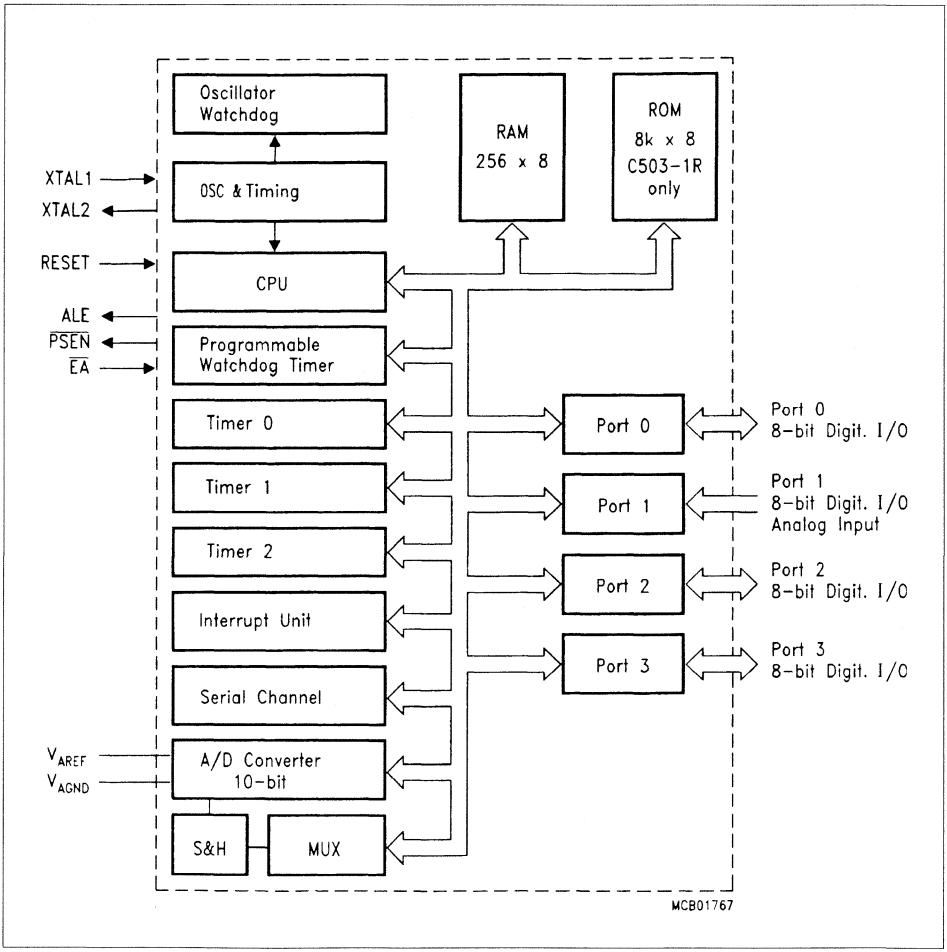


Figure 1: Block Diagram of the SAB-C503

CPU

The SAB-C503 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions executed in 1.0 µs (20 MHz : 600 ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. 0D0H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxiliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address 00H - 07H
0	1	Bank 1 selected, data address 08H - 0FH
1	0	Bank 2 selected, data address 10H - 17H
1	1	Bank 3 selected, data address 18H - 1FH
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag.** Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 33 special function registers (SFRs) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in table 1, table 2 and table 3.

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB-C503. Table 3 illustrates the contents of the SFRs.

Table 1, Special Function Registers in numeric order of their addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXH [2]
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	(WDTL) [3]	00H	9CH	reserved	XXH [2]
85H	(WDTH) [3]	00H	9DH	reserved	XXH [2]
86H	WDTREL	00H	9EH	reserved	XXH [2]
87H	PCON	000X0000B [2]	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IE** [1]	**00H**
91H	reserved	00H	A9H	reserved	XXH [2]
92H	reserved	XXH [2]	AAH	reserved	XXH [2]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved
[3]: () ... SFR not user accessable

Table 1, Special Function Register in numeric order of their addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3** [1]	)0FFH	**D8H**	**ADCON0** [1]	00H
B1H	reserved	XXH [2]	D9H	ADDATH	00H
B2H	reserved	XXH [2]	DAH	ADDATL	00H
B3H	reserved	XXH [2]	DBH	reserved	XXH [2]
B4H	reserved	XXH [2]	DCH	ADCON1	0XXXX000B [2]
B5H	reserved	XXH [2]	DDH	reserved	XXH [2]
B6H	reserved	XXH [2]	DEH	reserved	XXH [2]
B7H	reserved	XXH [2]	DFH	reserved	XXH [2]
B8H	**IP** [1]	**X0000000B** [2]	**E0H**	**ACC** [1]	**00H**
B9H	reserved	XXH [2]	E1H	reserved	XXH [2]
BAH	reserved	XXH [2]	E2H	reserved	XXH [2]
BBH	reserved	XXH [2]	E3H	reserved	XXH [2]
BCH	reserved	XXH [2]	E4H	reserved	XXH [2]
BDH	reserved	XXH [2]	E5H	reserved	XXH [2]
BEH	reserved	XXH [2]	E6H	reserved	XXH [2]
BFH	reserved	XXH [2]	E7H	reserved	XXH [2]
C0H	**WDCON** [1]	**XXXX0000B** [2]	**E8H**	reserved	XXH [2]
C1H	reserved	XXH [2]	E9H	reserved	XXH [2]
C2H	reserved	XXH [2]	EAH	reserved	XXH [2]
C3H	reserved	XXH [2]	EBH	reserved	XXH [2]
C4H	reserved	XXH [2]	ECH	reserved	XXH [2]
C5H	reserved	XXH [2]	EDH	reserved	XXH [2]
C6H	reserved	XXH [2]	EEH	reserved	XXH [2]
C7H	reserved	XXH [2]	EFH	reserved	XXH [2]
C8H	**T2CON** [1]	**00H**	**F0H**	**B** [1]	**00H**
C9H	T2MOD	XXXXXXX0B [2]	F1H	reserved	XXH [2]
CAH	RC2L	00H	F2H	reserved	XXH [2]
CBH	RC2H	00H	F3H	reserved	XXH [2]
CCH	TL2	00H	F4H	reserved	XXH [2]
CDH	TH2	00H	F5H	reserved	XXH [2]
CEH	reserved	XXH [2]	F6H	reserved	XXH [2]
CFH	reserved	XXH [2]	F7H	reserved	XXH [2]
D0H	**PSW** [1]	**00H**	**F8H**	reserved	**XXH** [2]
D1H	reserved	XXH [2]	F9H	reserved	XXH [2]
D2H	reserved	XXH [2]	FAH	reserved	XXH [2]
D3H	reserved	XXH [2]	FBH	reserved	XXH [2]
D4H	reserved	XXH [2]	FCH	reserved	XXH [2]
D5H	reserved	XXH [2]	FDH	reserved	XXH [2]
D6H	reserved	XXH [2]	FEH	reserved	XXH [2]
D7H	reserved	XXH [2]	FFH	reserved	XXH [2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved

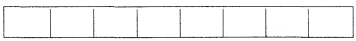
Table 2, Special Function Registers - Functional blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H** [1]	00H
	B	B-Register	**0F0H** [1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**0D0H** [1]	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	**0A8H** [1]	00H
	IP	Interrupt Priority Register	**0B8H** [1]	00H
Ports	P0	Port 0	**80H** [1]	0FFH
	P1	Port 1, Analog/Digital Input	**90H** [1]	0XXH [3]
	P2	Port 2	**0A0H** [1]	0FFH
	P3	Port 3	**0B0H** [1]	0FFH
A/D-Converter	ADCON0	A/D Converter Control Register 0	**0D8H** [1]	00H
	ADCON1	A/D Converter Control Register 1	0DCH	0XXX X000B [3]
	ADDATH	A/D Converter Data Register High Byte	0D9H	00H
	ADDATL	A/D Converter Data Register Low Byte	0DAH	00H
Serial Channels	PCON [2]	Power Control Register	87H	00H
	SBUF	Serial Channel Buffer Reg.	99H	0XXH [3]
	SCON	Serial Channel 0 Control Reg.	**98H** [1]	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88H** [1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	**0C8H** [1]	00H
	T2MOD	Timer 2 Mode Register	0C9H	XXXX XXX0B [3]
	RC2H	Timer 2 Reload Capture Reg., High Byte	0CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
Watchdog	WDCON	Watchdog Timer Control Register	**0C0H** [1]	XXXX 0000B [3]
	WDTREL	Watchdog Timer Reload Reg.	86H	00H
Pow.Sav. Modes	PCON	Power Control Register	87H	000X0000B [3]

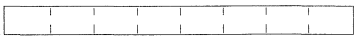
[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks
[3] X means that the value is indeterminate and the location is reserved

Table 3, Contents of SFRs, SFRs in numeric order

Address	Register	Bit 7	6	5	4	3	2	1	0
80H	P0								
81H	SP								
82H	DPL								
83H	DPH								
86H	WDTREL								
87H	PCON	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
8AH	TL0								
8BH	TL1								
8CH	TH0								
8DH	TH1								
90H	P1								
98H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99H	SBUF								
A0H	P2								
A8H	IE	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
B0H	P3								
B8H	IP	–	PADC	PT2	PS	PT1	PX1	PT0	PX0
C0H	WDCON	–	–	–	–	OWDS	WDTS	WDT	SWDT
C8H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
C9H	T2MOD	–	–	–	–	–	–	–	DCEN



SFR bit and byte addressable



SFR not bit addressable

must not be used

– : = bit location is reserved

Table 3, Contents of SFRs, SFRs in numeric order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
CAH	RC2L								
CBH	RC2H								
CCH	TL2								
CDH	TH2								
D0H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
D8H	ADCON0	–	–	IADC	BSY	ADM	MX2	MX1	MX0
D9H	ADDATH	MSB							
DAH	ADDATL		LSB	–	–	–	–	–	–
DCH	ADCON1	ADCL	–	–	–	MX3	MX2	MX1	MX0
E0H	ACC								
F0H	B								

SFR bit and byte addressable

SFR not bit addressable

must not be used

– : = bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in table 4:

Table 4, Timer/Counter 0 and 1 operating modes

Mode	Description	TMOD				Input clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/12 \times 32$	$f_{OSC}/24 \times 32$
1	16-bit timer/counter	X	X	0	1	$f_{OSC}/12$	$f_{OSC}/24$
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	$f_{OSC}/12$	$f_{OSC}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$

In the "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. Figure 2 illustrates the input clock logic.

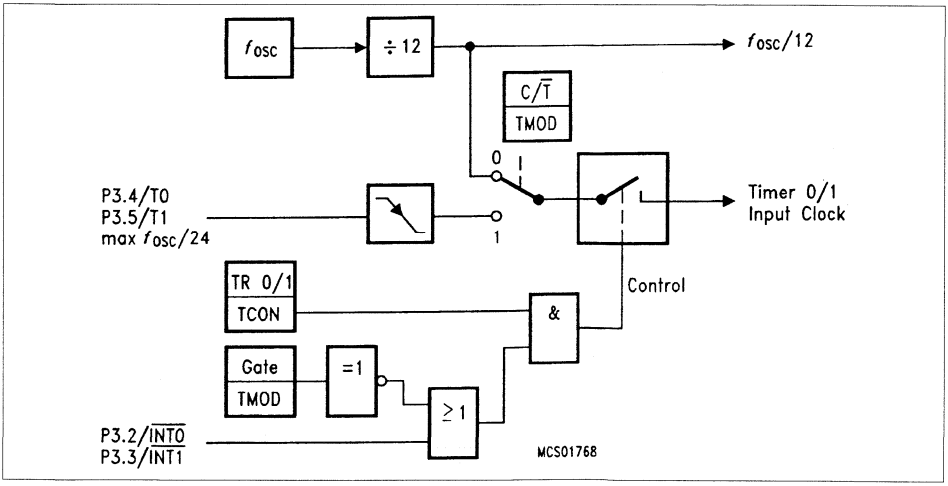


Figure 2, Timer/Counter 0 and 1 input clock logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5, Timer/Counter 2 operating modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ $\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{OSC}/12$	max $f_{OSC}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	$f_{OSC}/12$	max $f_{OSC}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$f_{OSC}/2$	max $f_{OSC}/24$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in table 6. The possible baudrates can be calculated using the formulas given in table 7.

Table 6, USART operating modes

Mode	T2CON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bits are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7, Formulas for calculating Baudrates

Baud rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate$) /32$ $(2^{SMOD} \times f_{OSC}) / (32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	f_{OSC} / (32 × (65536-(RC2H, RC2L))

10-bit A/D Converter

In the SAB-C503 a high performance/high speed 8-channel 10-bit A/D-Converter (ADC) using the successive approximation technique is implemented.

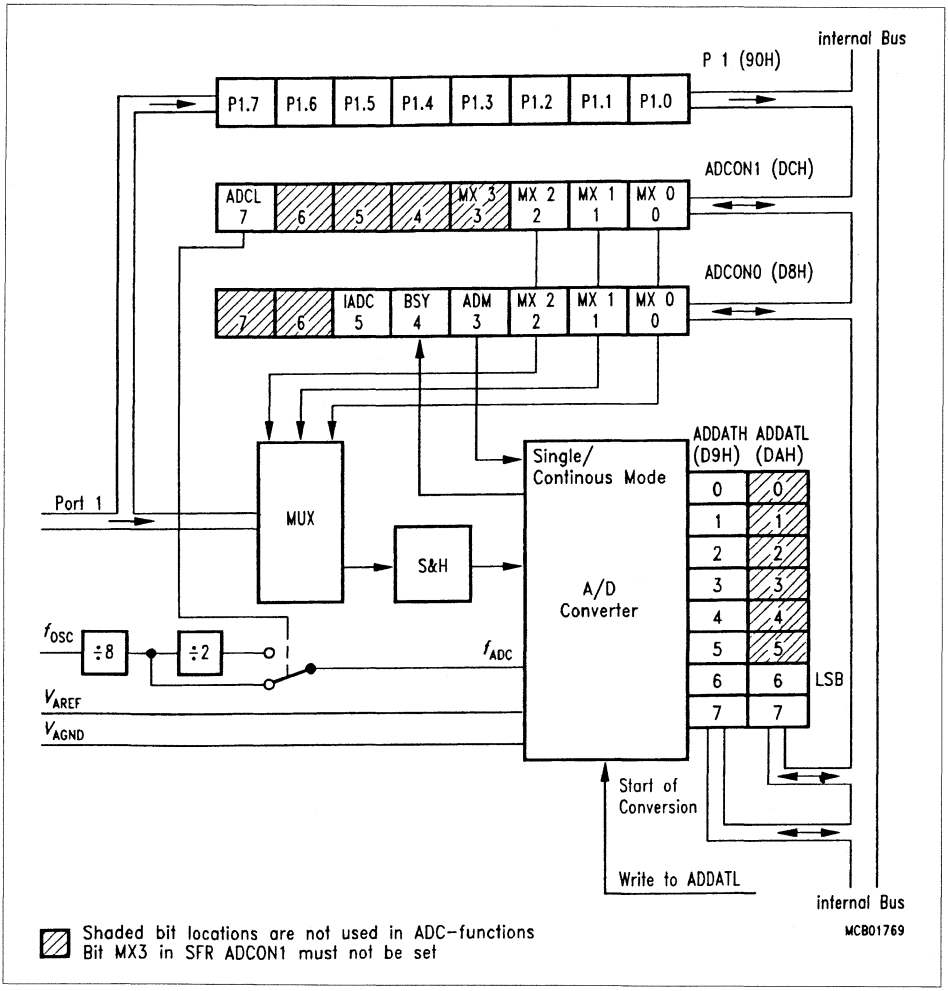


Figure 3, Block Diagram A/D-Converter

Note that bit ADCL in SFR ADCON0 has to be set when f_{OSC} is higher than 16 MHz. Furthermore bit MX3 in SFR ADCON1 must not be set otherwise a not connected channel would be selected.

The formula for the conversion time is given by: $t_C = 14 \times (8 \times 2^{ADCL}) / f_{OSC}$

Interrupt System

The SAB-C503 provides 7 interrupt sources with two priority levels. Figure 4 gives a general overview of the interrupt sources and illustrates the request and control flags.

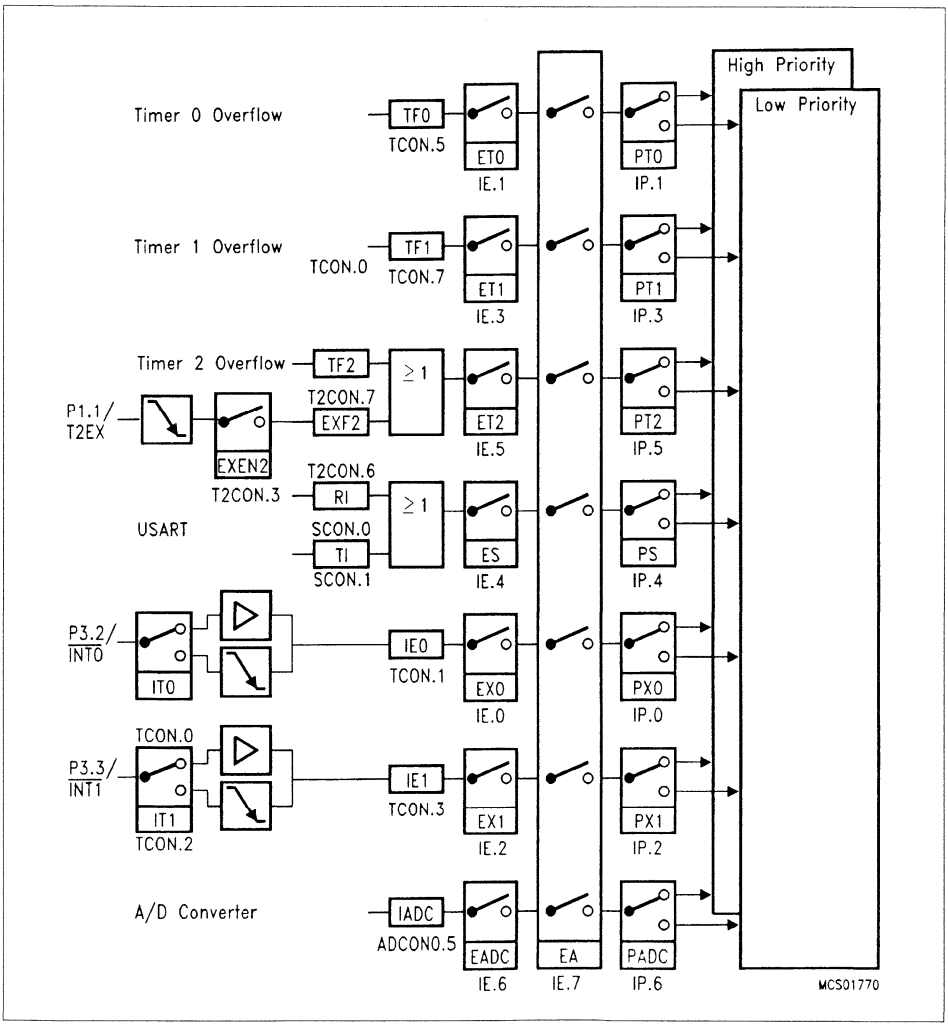


Figure 4, Interrupt Request Sources

Table 8, Interrupt sources and their corresponding interrupt vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in table 9.

Table 9, Interrupt priority-within-level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
A/D Converter,	IADC	
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI or TI	
Timer 2 Interrupt,	TF2 or EXF2	Low

Fail Safe Mechanismus

The SAB-C503 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure.

1) Watchdog Timer (15bit, WDT)
2) Oscillator Watchdog (OWD)

1) Watchdog Timer (WDT)

The Watchdog Timer in the SAB-C503 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler. The latter is enabled by setting bit WDTREL.7.

Figure 5 shows the block diagram of the programmable Watchdog Timer.

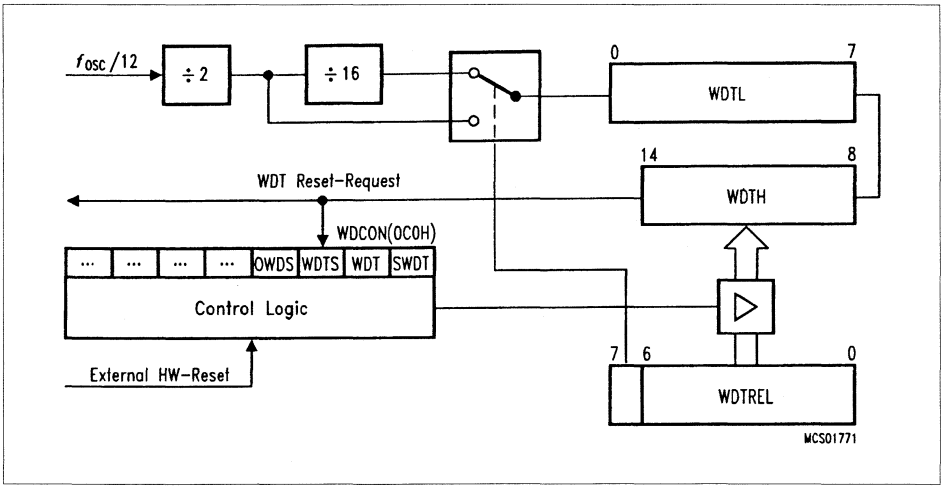


Figure 5, Block Diagram of the Programmable Watchdog Timer

– Starting and refreshing the WDT

Table 10 gives an overview how to start and refresh the WDT. The mentioned bits are located in SFR WDCON.

Table 10, Starting and refreshing the WDT

Function	Example	Remarks
Starting WD	SETB SWDT	Cannot be stopped during active mode of the device. WDT is halted during idle mode, power down mode or the oscillator watchdog reset is active.
Refreshing WD	SETB WDT SETB SWDT	Double instruction sequence (setting bit WDT and SWDT consecutively) to increase system security.

– Watchdog reset and watchdog status flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state 7FFCH. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS (SFR WDCON) is set. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

2) Oscillator Watchdog (OWD)

The OWD consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

Figure 6 shows the block diagram of the oscillator watchdog unit while table 11 shows the effect when the OWD becomes activ/inactiv

Note: The OWD is always enabled!

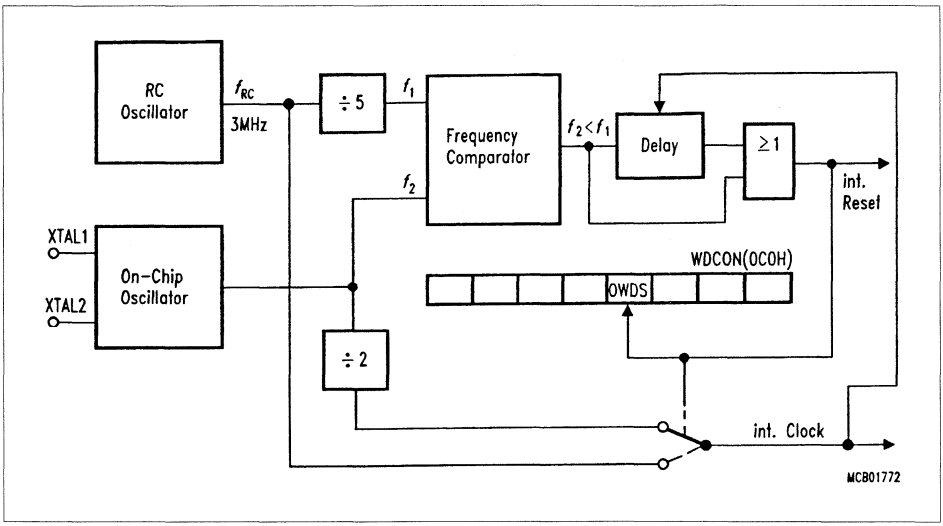


Figure 6, Functional Block Diagram of the Oscillator Watchdog

Table 11, Effects of the OWD

Conditions	Effect
$f_{OSC} < f_{RC}/5$	Switch input of internal clock system to RC oscillator output Activating internal reset at the same time (reset sequence is clocked by RC-oscillator). Exception from effects of a Hardware Reset: Watchdog Timer Status Flag, WDTS is not reset Oscillator Watchdog Status Flag, OWDS is set
$f_{OSC} > f_{RC}/5$	Input of internal clock system is $f_{OSC}/2$. When failure condition ($f_{OSC} < f_{RC}/5$) disappears the part executes a final reset phase of typ. 1 ms in order to allow the external oscillator to stabilize.

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE, PDS and IDLE, IDLS select the Power Down mode or the idle mode, respectively. If the Power Down mode and the idle mode are set at the same time, Power Down takes precedence. Table 10 gives a general overview of the power saving modes.

Table 10, Power Saving modes overview

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active Double instruction sequence
Power-Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator are stopped. Contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR's contents). Double instruction sequence

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (simulator to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	– 40 to + 85 °C
Storage temperature (T_{ST})	– 65 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 V to V_{CC} + 0.5 V
Input current on any pin during overload condition	– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition	| 100 mA |
Power dissipation	TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 °C to 70 °C for the SAB-C503
T_A = – 40 °C to 85 °C for the SAF-C503

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except RESET, XTAL1, $\overline{EA}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to RESET, $\overline{EA}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, P1)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 20 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 20 MHz [7]	I_{CC}	–	TBD	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V, [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = RESET = Port 0 = Port 1 = V_{CC}; XTAL2 = N.C.; XTAL1 = V_{SS}; V_{AGND} = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V, XTAL2 = N.C.; $\overline{EA}$ = Port 0 = Port 1 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.; RESET = $\overline{EA}$ = V_{SS}; Port 0 = Port 1 = V_{CC}; all other pins are disconnected;

7) $I_{CC\,Max}$ other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;

T_A = 0 °C to 70 °C for the SAB-C503
T_A = – 40 °C to 85 °C for the SAF-C503

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (Inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY} [1]	µs	[3]
Total unadjusted error [4]	TUE			± 2	LSB	VAREF = V_{CC} VAGND = V_{SS}

[1] $t_{CY} = (8 \times 2^{ADCL}) / f_{OSC}$ ($t_{CY} = 1 / f_{ADC}$; $f_{ADC} = f_{OSC} / (8 \times 2^{ADCL})$)

[2] This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4 TCY is 2 µs at the f_{OSC} = 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.

[3] This parameter includes the sample time T_S. 14 TCY is 7 µs at f_{OSC} = 16 MHz.

[4] This parameter includes also the DNLE.

AC Characteristics for SAB-C503-LN / C503-1RN

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C503
T_A = – 40 °C to 85 °C for the SAF-C503

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	60	–	$t_{CLCL} - 23$	–	ns
Address to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C503 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C503-LN / C503-1RN

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C503-L20N / C503-1R20N

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C503
T_A = – 40 °C to 85 °C for the SAF-C503

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
Address to valid instr in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C503 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

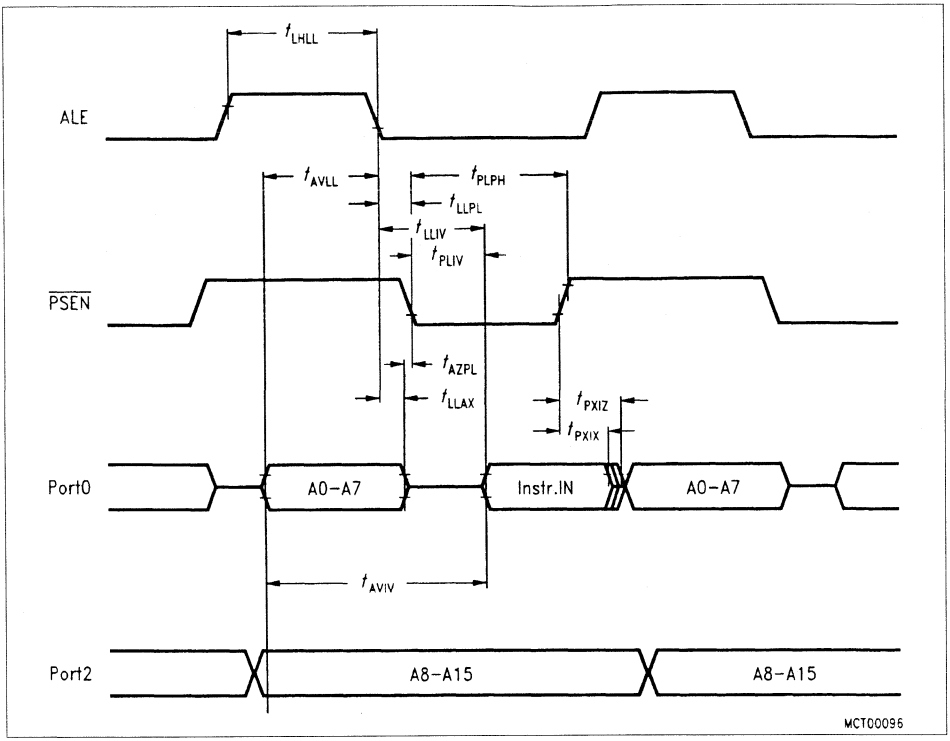
AC Characteristics for SAB-C501-L20N / C503-1R20N

External Data Memory Characteristics

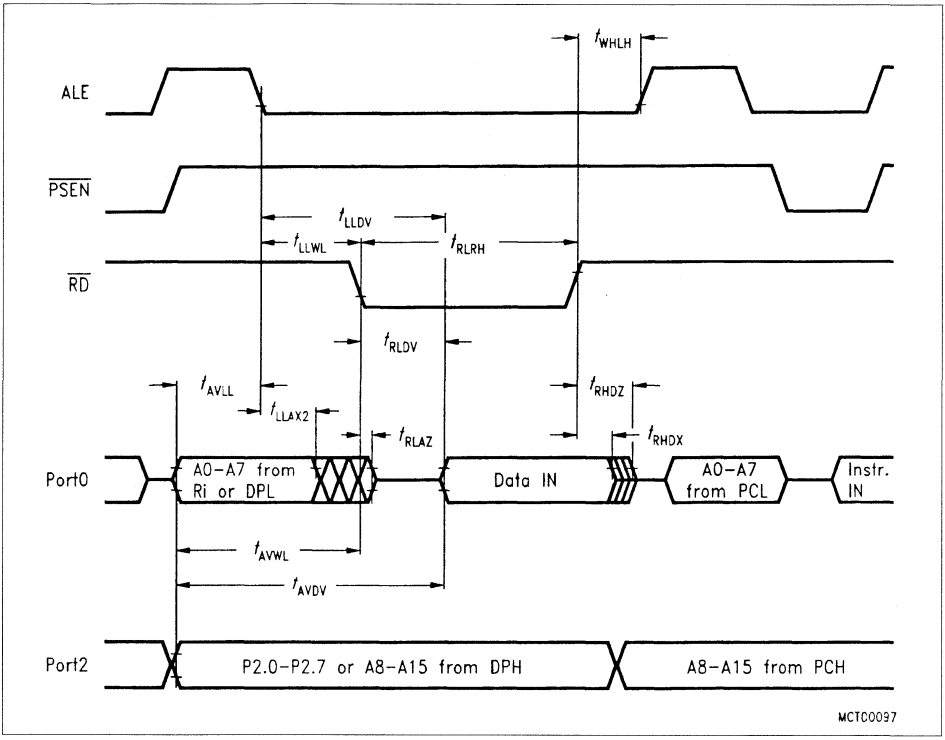
Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	65	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	40	–	$2t_{CLCL} - 60$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

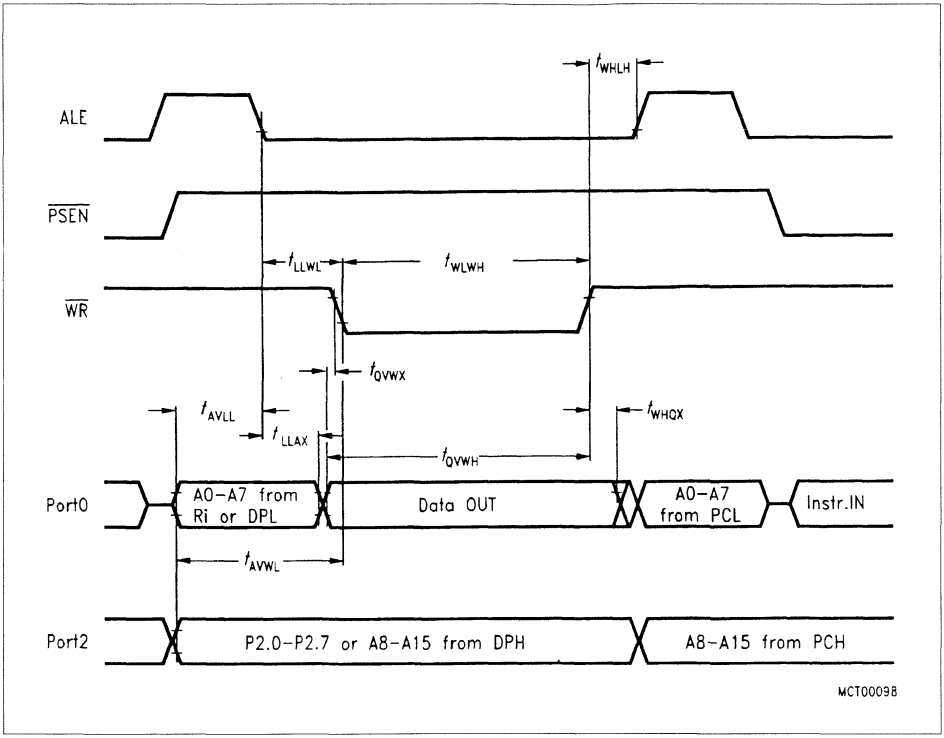
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



Program Memory Read Cycle



Data Memory Read Cycle

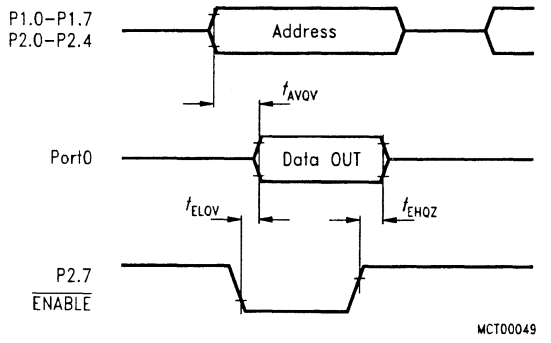


Data Memory Write Cycle

ROM Verification Characteristics for SAB-C503-1R

ROM Verification Mode 1

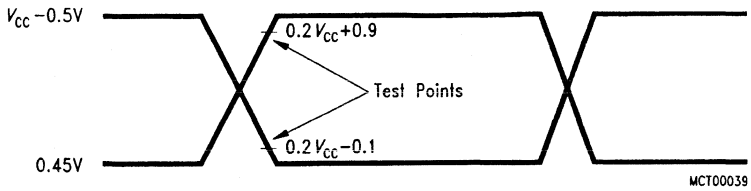
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

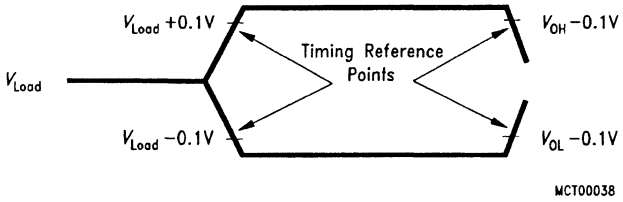
Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

ROM Verification Mode 1



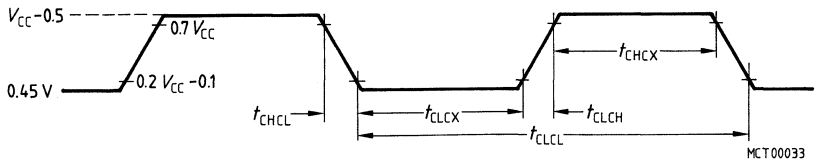
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms

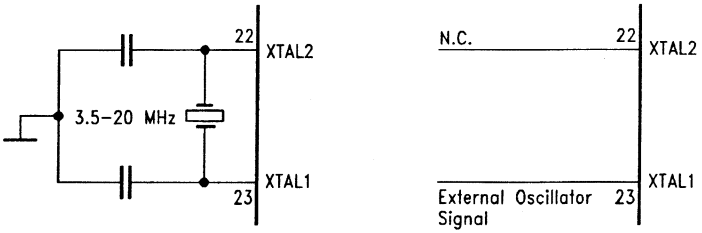


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs. I_{OL} / $I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



External Clock Cycle



C = 30pF ± 10pF
(incl. stray capacitance)

Crystal Oscillator Mode

Driving from External Source

Recommended Oscillator Circuits

16-Bit Single-Chip Microcontrollers

SIEMENS

High-Performance 16-Bit CMOS Single-Chip Microcontrollers for Embedded Control Applications

SAB 80C166/83C166

Advance Information

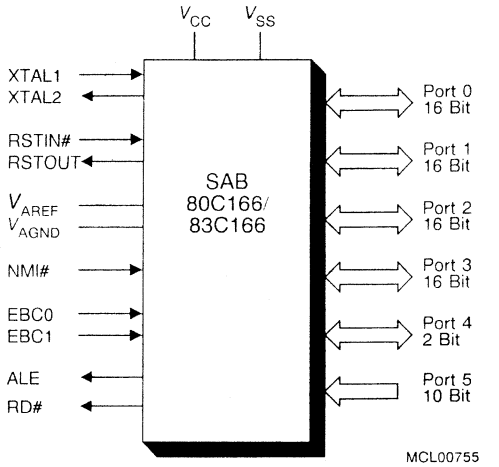
SAB 83C166-3S 16-bit Microcontroller with 8K Mask-Programmable ROM
SAB 80C166-S 16-bit Microcontroller for External Program Memory

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU clock
- 500 ns Multiplication (16×16 bits), 1 µs Division (32-/16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- 256 Kbytes Linear Address Space for Code and Data
- 1 Kbyte On-Chip RAM
- 8 Kbytes On-Chip ROM (for the SAB 83C166, only)
- 512 bytes On-Chip Special Function Register Area
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System
- 10-Channel 10-bit A/D Converter with 9.75 µs Conversion Time
- 16-Channel Capture/Compare Unit
- 2 Multi-Functional General Purpose Timer Units
- 2 Serial Channels (USARTs)
- Programmable Watchdog Timer
- 76 General Purpose I/O Lines
- Temperature Range: 0 to 70 °C (in preparation: – 40 to 85 °C, – 40 to 110 °C)
- 1.2 micron Siemens Low-Power CMOS Process
- Complete Set of Development Tools 'C'-Compiler, Macro Assembler, Linker, Locater, Librarian, Simulator, Emulator, Evaluation Board
- 100 Pin Plastic Quad Flat Pack (PQFP) Package

Introduction

The SAB 80C166 and the SAB 83C166 are the first representatives of the new Siemens SAB 80C166 family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 10 million instructions per second) with high peripheral functionality.

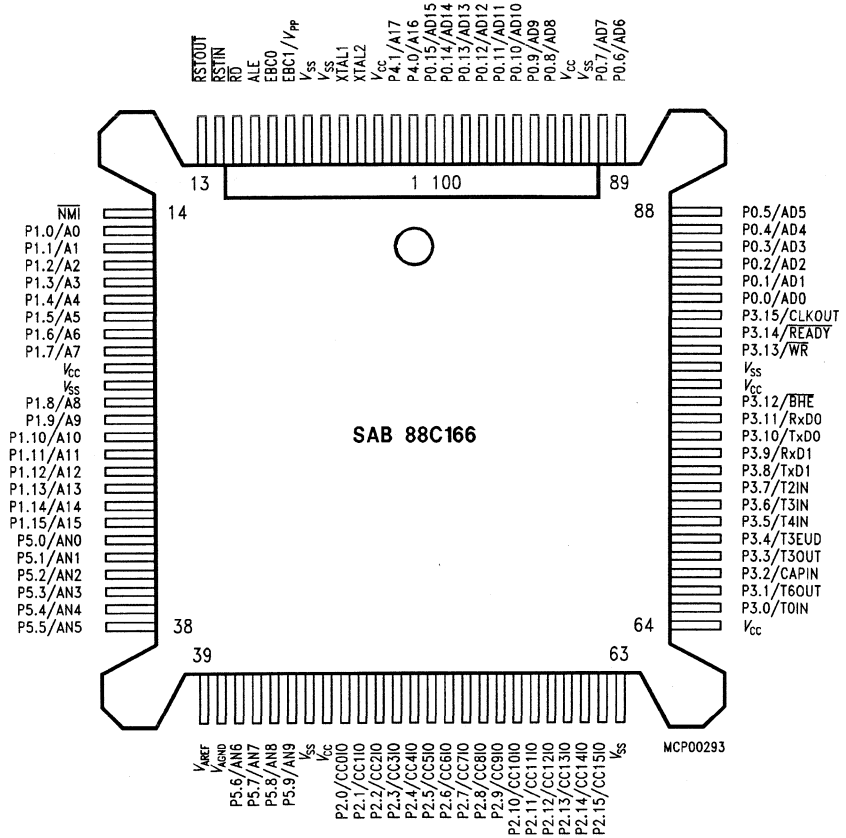
Figure 1
Logic Symbol



Ordering Information

Type	Ordering Code	Package	Descriptions
16-bit Single-Chip Microcontroller			
SAB 80C166-S	Q67120-C493	P-BQFP-100	for external memory,20 MHz
SAB 80C166-M	Q67120-C848	P-MRFP-100	
SAB 83C166-5S	Q67120-C567	P-BQFP-100	with factory mask-programmable ROM, 20 MHz
SAB 83C166-5M	Q67120-C849	P-MRFP-100	
SAB 80C166-S-T3	Q67120-C794	P-BQFP-100	for external memory,20 MHz, ext. temp. -40 °C to 85 °C
SAB 80C166-M-T3	Q67120-C900	P-MRFP-100	
SAB 83C166-5S-T3	Q67120-C912	P-BQFP-100	with factory mask-programmable ROM,20 MHz, ext. temp. -40 °C to 85 °C
SAB 83C166-5M-T3	Q67120-C911	P-MRFP-100	

Figure 2
Pin Configuration (Top View)



Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
P4.0 - P4.1	1.2	I/O	Port 4 is a 2-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 is used for output of the two segment address lines supposed that segmentation is enabled: P4.0 A16 Lower segment address line P4.1 A17 Higher segment address line
	1 2	O O	
XTAL1	5	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	4	O	XTAL2: Output of the oscillator amplifier circuits. To drive the device from an external source, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
EBC0 EBC1	9 8	I I	External Bus Configuration selection inputs. These pins are sampled during reset and select either the single chip mode or one of the three external bus configurations, as follows: EBC1 EBC0 Mode Bus Configuration 0 0 Single Chip Mode 1 1 16/18-bit addresses, 8-bit data, multiplexed bus 1 0 16/18-bit addresses, 16-bit data, multiplexed bus 1 1 16/18-bit addresses, 16-bit data, non-multiplexed bus
RSTIN#	12	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the SAB 80C166/83C166. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
RSTOUT#	13	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. RSTOUT# remains low until the EINIT (end of initialization) instruction is executed.
NMI#	14	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI# pin must be low in order to force the SAB 80C166/83C166 to go into power down mode. If NMI# is high when PWRDN is executed, the part will continue to run in normal mode.
ALE	10	O	Address latch enable output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
RD#	11	O	External memory read control signal. RD# is activated for every external instruction or data read access.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
P1.0 - P1.15	15 - 22 25 - 32	I/O	Port 1 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. Port 1 is also used as the 16-bit address bus (A) in the non- multiplexed bus mode.
	15 - 22 25 - 32	O O	16-bit address bus, non multiplexed: P1.0 - P1.15 A0 - A15
P5.0 - P5.9	33 - 38 41 - 44	I I	Port 5 is a 10-bit input port with Schmitt-Trigger characteristics. The pins of Port 5 are also used as the analog input channels for the A/D converter as listed below:
	33	I	P5.0 AN0 Analog input channel 0
	34	I	P5.1 AN1 Analog input channel 1
	35	I	P5.2 AN2 Analog input channel 2
	36	I	P5.3 AN3 Analog input channel 3
	37	I	P5.4 AN4 Analog input channel 4
	38	I	P5.5 AN5 Analog input channel 5
	41	I	P5.6 AN6 Analog input channel 6
	42	I	P5.7 AN7 Analog input channel 7
	43	I	P5.8 AN8 Analog input channel 8
	44	I	P5.9 AN9 Analog input channel 9
P2.0 - P2.15	47 - 62	I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. The pins of Port 2 are also used as the capture inputs or compare outputs for the CAPCOM unit as listed in the following table:
	47	I/O	P2.0 CC0IO Register CC0 capture input/compare output
	48	I/O	P2.1 CC1IO Register CC1 capture input/compare output
	49	I/O	P2.2 CC2IO Register CC2 capture input/compare output
	50	I/O	P2.3 CC3IO Register CC3 capture input/compare output
	51	I/O	P2.4 CC4IO Register CC4 capture input/compare output
	52	I/O	P2.5 CC5IO Register CC5 capture input/compare output
	53	I/O	P2.6 CC6IO Register CC6 capture input/compare output
	54	I/O	P2.7 CC7IO Register CC7 capture input/compare output
	55	I/O	P2.8 CC8IO Register CC8 capture input/compare output
	56	I/O	P2.9 CC9IO Register CC9 capture input/compare output
	57	I/O	P2.10 CC10IO Register CC10 capture input/compare output
	58	I/O	P2.11 CC11IO Register CC11 capture input/compare output
	59	I/O	P2.12 CC12IO Register CC12 capture input/compare output
	60	I/O	P2.13 CC13IO Register CC13 capture input/compare output
	61	I/O	P2.14 CC14IO Register CC14 capture input/compare output
	62	I/O	P2.15 CC15IO Register CC15 capture input/compare output
P3.0 - P3.15	65-77 80-82	I/O I/O	Port 3 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. The pins of Port 3 are also used for various functions such as timer inputs and outputs and bus control signals. The alternate functions of the Port 3 pins are listed in the following:

Pin Definitions and Functions (cont'd)

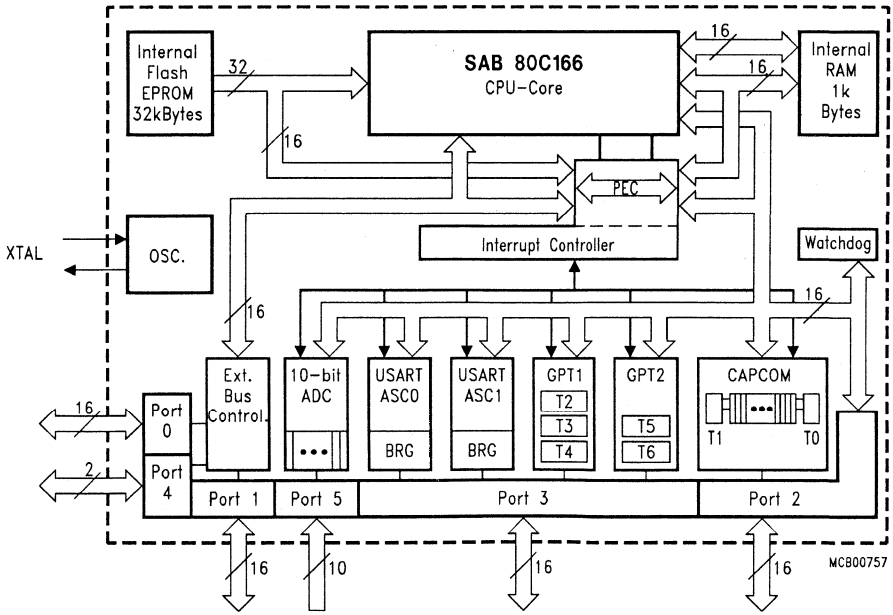
Symbol	Pin Number	Input (I) Output (O)	Function		
P3.0 - P3.15 (cont'd)	65	I	P3.0	T0IN	Timer 0 count input
	66	O	P3.1	T6OUT	Timer 6 toggle latch output
	67	I	P3.2	CAPIN	CAPREL register capture input
	68	O	P3.3	T3OUT	Timer 3 toggle latch output
	69	I	P3.4	T3EUD	Timer 3 external up/down control input
	70	I	P3.5	T4IN	Timer 4 count/gate/reload/capture input
	71	I	P3.6	T3IN	Timer 3 count/gate/input
	72	I	P3.7	T2IN	Timer 2 count/gate/reload/capture input
	73	O	P3.8	TxD1	Serial Channel 1 clock output in synchronous mode; data output in asynchronous mode
	74	I/O	P3.9	RxD1	Serial Channel 1 data input/output in synchronous mode; data input in asynchronous mode
	75	O	P3.10	T×D0	Serial Channel 0 clock output in synchronous mode; data output in asynchronous mode
	76	I/O	P3.11	R×D0	Serial Channel 0 data input/output in synchronous mode; data input in asynchronous mode
	77	O	P3.12	BHE#	External memory byte enable control signal
	80	O	P3.13	WR#	External memory write control signal
	81	I	P3.14	READY#	Ready input
	82	O	P3.15	CLKOUT	System clock output (oscillator frequency/2)
P0.0 - P0.15	83 - 90 93 - 100	I/O O	Port 0 is a 16-bit bidirectional I/O port. In case of the Single Chip Mode, Port 0 is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 0 serves as the address (A) and address/data (AD) bus in the multiplexed bus modes and as the data (D) bus in the non-multiplexed bus mode.		
			16-/18-bit addresses, 8-bit data, multiplexed bus:		
	83 - 90	I/O	P0.0 - P0.7	AD0 - AD7	
	93 - 100	O	P0.8 - P0.15	A8 - A15	
			16-/18-bit addresses, 16-bit data, multiplexed bus:		
	83 - 90 93 - 100	I/O	P0.0 - P0.15	AD0 - AD15	
			16-/18-bit addresses, 16-bit data, non-multiplexed bus:		
	83 - 90 93 - 100	I/O	P0.0 - P0.15	D0 - D15	
V_{CC}	3, 23, 46, 64 78, 92		Digital supply voltage: + 5 V during normal operation and idle mode ≥ 2.5 V during power down mode		
V_{SS}	6, 7, 24 45, 63, 79, 91		Digital ground		
V_{AREF}	39		Reference voltage for the A/D converter		
V_{AGND}	40		Reference ground for the A/D converter		

Functional Description

The architecture of the SAB 80C166 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the SAB 80C166.

Note: In this description, any reference to the SAB 80C166 also applies to the SAB 83C166 unless otherwise noted. All time specifications refer to a CPU clock of 20 MHz which means an oscillator frequency (f_{OSC}) of 40 MHz.

Figure 3
Block Diagram



Memory Organization

The memory space of the SAB 80C166 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which currently includes 256 Kbytes. Address space expansion to 16 Mbytes is provided for future versions. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

The SAB 83C166 contains 8 Kbytes of a mask-programmable on-chip ROM for code or constant data.

A large dual port RAM of 1 Kbyte is contained on both the SAB 80C166 and the SAB 83C166. This internal RAM is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, . . ., RL7, RH7) so called General Purpose Registers (GPRs).

512 bytes of the address space are reserved for the Special Function Register (SFR) area. SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. 98 SFRs are currently implemented. Unused SFR addresses are reserved for future members of the SAB 80C166 family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 256 Kbytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed to either the Single Chip Mode when no external memory is required, or to one of three different external memory access modes, which are as follows:

– 16-/18-bit Addresses, 16-bit Data, Non-Multiplexed

– 16-/18-bit Addresses, 16-bit Data, Multiplexed

– 16-/18-bit Addresses, 8-bit Data, Multiplexed

In the non-multiplexed bus mode, Port 1 is used as an output for addresses and Port 0 is used as an input/output for data. In the multiplexed bus modes, just one of the two 16-bit ports, Port 0, is used as an input/output for both addresses and data.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time and Read write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories. Access to very slow memories is supported via a particular 'Ready' function.

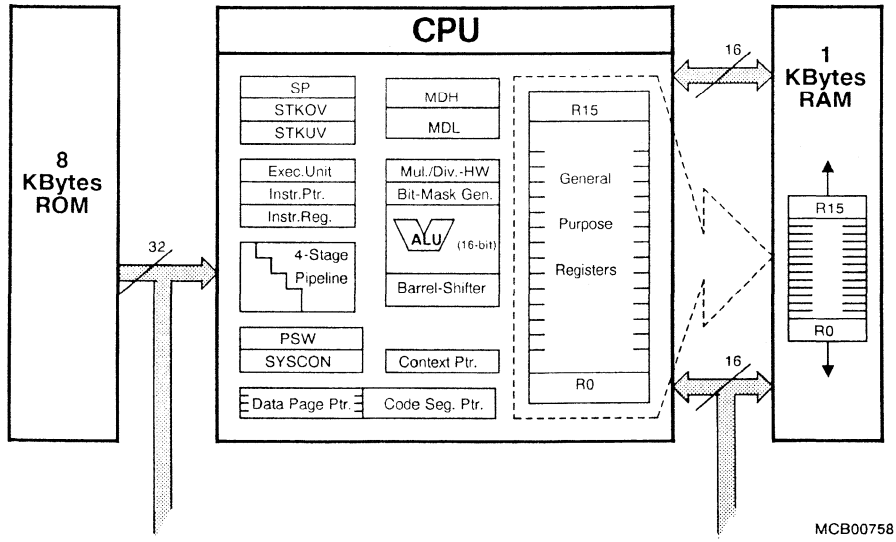
For applications which require less than 64 Kbytes of memory space, a non-segmented memory model can be selected. In this case, all memory locations can be addressed by 16 bits, and thus Port 4 is not needed as an output for the two most significant address bits (A17 and A16), as is the case when using the segmented memory model.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the SAB 80C166's instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: A 32-/16 bit division in 1 µs, a
16 × 16 bit multiplication in 0.5 µs, and branches in 200 ns. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 200 ns to 100 ns.

Figure 4
CPU Block Diagram



The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at the time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, register banks can also be organized overlappingly.

A system stack of up to 512 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly functional SAB 80C166 instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the SAB 80C166 is capable of reacting very fast to the occurence of non-deterministic events.

The architecture of the SAB 80C166 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data, or for transferring A/D converted results to a memory table. The SAB 80C166 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized servise request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible SAB 80C166 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	40h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	44h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	48h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	4Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	50h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	54h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	58h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	5Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	60h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	64h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	68h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	6Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	70h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	74h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	78h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	7Ch	1Fh
CAPCOM Timer 0	T0IR	T0IE	T0INT	80h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	84h	21h
GPT 1 Timer 2	T2IR	T2IE	T2INT	88h	22h
GPT 1 Timer 3	T3IR	T3IE	T3INT	8Ch	23h
GPT 1 Timer 4	T4IR	T4IE	T4INT	90h	24h
GPT 2 Timer 5	T5IR	T5IE	T5INT	94h	25h
GPT 2 Timer 6	T6IR	T6IE	T6INT	98h	26h
GPT 2 CAPREL Register	CRIR	CRIE	CRINT	9Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	A4h	29h
Serial Channel 0 Tansmit	S0TIR	S0TIE	S0TINT	A8h	2Ah
Serial Channel 0 Receive	S0RIR	S0RIE	S0RINT	ACh	2Bh
Serial Channel 0 Error	S0EIR	S0EIE	S0EINT	B0h	2Ch
Serial Channel 1 Transmit	S1TIR	S1TIE	S1TINT	B4h	2Dh
Serial Channel 1 Receive	S1RIR	S1RIE	S1RINT	B8h	2Eh
Serial Channel 1 Error	S1EIR	S1EIE	S1EINT	BCh	2Fh

The SAB 80C166 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'HardwareTraps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location).
The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except another higher prioritized trap service being in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:					
Hardware Reset		RESET	0h	0h	III
Software Reset		RESET	0h	0h	III
Watchdog Timer Overflow		RESET	0h	0h	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	08h	2h	II
Stack Overflow	STKOF	STOTRAP	10h	4h	II
Stack Underflow	STKUF	STUTRAP	18h	6h	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	28h	Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	28h	Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	28h	Ah	I
Illegal Instruction Access	ILLINA	BTRAP	28h	Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	28h	Ah	I
Reserved			[2Ch - 3Ch]	[Bh - Fh]	
Software Traps TRAP Instruction			Any [0h - 1FCh] in steps of 4H	Any [0h - 7Fh]	Current CPU Priority

Capture/Compare (CAPCOM) Unit

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 400 ns. The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T0/T1) with reload registers provide two independent time bases for the capture/compare register array.

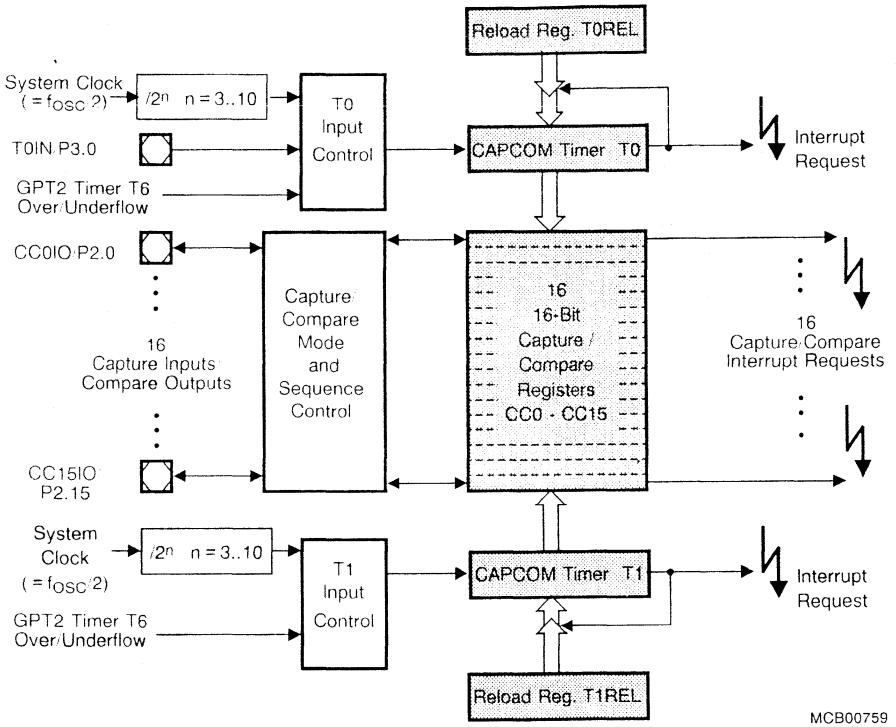
The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustment to the application specific requirements. In addition, an external count input for CAPCOM timer T0 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1, and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('capture'd) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set to '1' on match; pin reset to '0' on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

Figure 5
CAPCOM Unit Block Diagram



General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the internal system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (T2IN, T3IN, T4IN) which serves as gate or clock input. The maximum resolution of the timers in the GPT1 module is 400 ns ($@f_{OSC}$ = 40 MHz).

The count direction (up/down) for each timer is programmable by software. For timer T3, the count direction may additionally be altered dynamically by an external signal on a port pin (T3EUD) to facilitate e. g. position tracking.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over- flow/ underflow. The state of this latch may be output on a port pin (T3OUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 are captured into T2 or T4 in response to a signal at their associated input pins (T2IN, T4IN). Timer T3 is reloaded with the contents of T2 or T4 either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 200 ns ($@f_{OSC}$ = 40 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can independently count up or down, clocked with an input clock which is derived from a programmable prescaler.
Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Figure 6
Block Diagram of GPT1

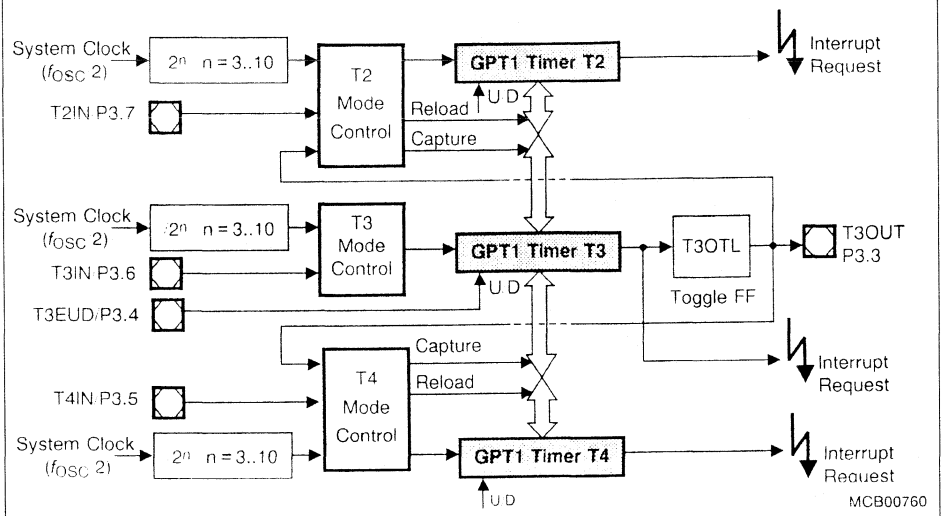
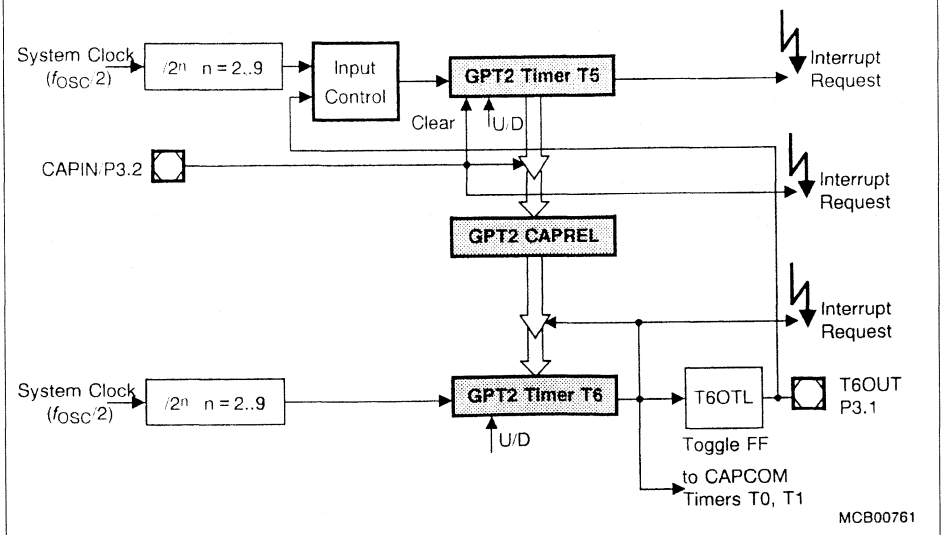


Figure 7
Block Diagram of GPT2



A/D Converter

For analog signal measurement, a 10-bit A/D converter with 10 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation which returns the conversion result for an analog channel within 9.75 µs ($@f_{OSC}$ = 40 MHz).

Overrun error detection capability is provided for the conversion result register (ADDAT): an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete.

For applications which require less than 10 analog input channels, the remaining channels can be used as digital input port pins.

The A/D converter of the SAB 80C166 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is once sampled and converted into a digital result. In the Single Channel Continuous mode, the analog level is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

Serial Channels

Serial communication with other microcontrollers, processors, terminals, or external peripheral components is provided by two serial interfaces with identical functionality, Serial Channel 0 (ASC0) and Serial Channel 1 (ASC1).

They are upward compatible with the serial ports of the Siemens SAB 8051x microcon- troller family and support full-duplex asynchronous communication up to 625 Kbaud and half-duplex synchronous communication up to 2.5 Mbaud.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In the synchronous mode, one data byte is transmitted or received synchronously to a shift clock which is generated by the SAB 80C166. In the asynchronous mode, an 8- or 9-bit data frame is transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode), and a loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmis- sion or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated if the last character received has not been read out of the receive buffer register at the time reception of a new character is complete.

Watchdog Timer

The Watchdog Timer of the SAB 80C166 represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer of the SAB 80C166 is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip'sstart-up procedure is always monitored. When the software has been designed to service the Watchdog Timer before it overflows, the Watchdog Timer times out if the program does not progress properly due to hardware or software related failures. When the Watchdog Timer overflows, it generates an internal hardware reset and pulls the RSTOUT# pin low in order to allow external hardware components to reset.

The Watchdog Timer of the SAB 80C166 is a 16-bit timer which can either be clocked with $f_{OSC}/4$ or $f_{OSC}/256$. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 µs and 420 ms can be monitored ($@f_{OSC}$ = 40 MHz). The default Watchdog Timer interval after reset is 6.55 ms.

Parallel Ports

The SAB 80C166 provides 76 I/O lines which are organized into four 16-bit I/O ports (Port 0 through 3), one 2-bit I/O port (Port 4), and one 10-bit input port (Port 5). All port lines are bit addressable, and all lines of Port 0 through 4 are individually bit-wise programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to the high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs.

Each port line has one programmable alternate input or output function associated with it. Ports 0 and 1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A16 and A17 in systems where segmentation is enabled to access more than 64 Kbytes of memory. Port 2 is associated with the capture inputs/compare outputs of the CAPCOM unit, and Port 3 includes alternate functions of timers, serial interfaces, optional bus control signals (WR#, BHE#, READY#), and the system clock output (CLKOUT). Port 5 is used for the analog input channels to the A/D converter. When anyone of these alternate functions is not used, the respective port line may be used as general purpose I/O line.

Special Function Registers Overview

The following table lists all SFRs which are implemented in the SAB 80C166 in alphabetical order. Bit-addressable SFRs are marked with the letter "b" in column "Name".
An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name	Physical Address	8-bit Address	Description	Reset Value
ADCIC b	FF98h	CCh	A/D Converter End of Conversion Interrupt Control Register	0000h
ADCON b	FFA0h	D0h	A/D Converter Control Register	0000h
ADDAT	FEA0h	50h	A/D Converter Result Register	0000h
ADEIC b	FF9Ah	CDh	A/D Converter Overrun Error Interrupt Control Register	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC0	FE80h	40h	CAPCOM Register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM Register 0 Interrupt Control Register	0000h
CC1	FE82h	41h	CAPCOM Register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM Register 1 Interrupt Control Register	0000h
CC2	FE84h	42h	CAPCOM Register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM Register 2 Interrupt Control Register	0000h
CC3	FE86h	43h	CAPCOM Register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM Register 3 Interrupt Control Register	0000h
CC4	FE88h	44h	CAPCOM Register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM Register 4 Interrupt Control Register	0000h
CC5	FE8Ah	45h	CAPCOM Register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM Register 5 Interrupt Control Register	0000h
CC6	FE8Ch	46h	CAPCOM Register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM Register 6 Interrupt Control Register	0000h
CC7	FE8Eh	47h	CAPCOM Register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM Register 7 Interrupt Control Register	0000h
CC8	FE90h	48h	CAPCOM Register 8	0000h
CC8IC b	FF88h	C4h	CAPCOM Register 8 Interrupt Control Register	0000h
CC9	FE92h	49h	CAPCOM Register 9	0000h
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h

Special Function Registers Overview (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CCM0 b	FF52h	A9h	CAPCOM Mode Control Register 0	0000h
CCM1 b	FF54h	AAh	CAPCOM Mode Control Register 1	0000h
CCM2 b	FF56h	ABh	CAPCOM Mode Control Register 2	0000h
CCM3 b	FF58h	ACh	CAPCOM Mode Control Register 3	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (2 bits, read only)	0000h
DP0 b	FF02h	81h	Port 0 Direction Control Register	0000h
DP1 b	FF06h	83h	Port 1 Direction Control Register	0000h
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	0000h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FF0Ah	85h	Port 4 Direction Control Register (2 bits)	0000h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (4 bits)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (4 bits)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (4 bits)	0002h
DPP3	FE06h	03h	CPU Data Page Pointer 3 Register (4 bits)	0003h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
ONES	FF1Eh	8Fh	Constand Value 1's Register (read only)	FFFFh

Special Function Registers Overview (cont'd)

Name		Physical Address	8-bit Address	Description	Reset Value
P0	**b**	FF00h	80h	Port 0 Register	0000h
P1	**b**	FF04h	82h	Port 1 Register	0000h
P2	**b**	FFC0h	E0h	Port 2 Register	0000h
P3	**b**	FFC4h	E2h	Port 3 Register	0000h
P4	**b**	FF08h	84h	Port 4 Register (2 bits)	0000h
P5	**b**	FFA2h	D1h	Port 5 Register (10 bits, read only)	XXXXh
PECC0		FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1		FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2		FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3		FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4		FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5		FECAh	65h	PEC Channel 5 Control Register	0000h
PECC6		FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7		FECEh	67h	PEC Channel 7 Control Register	0000h
PSW	**b**	FF10h	88h	CPU Program Status Word	0000h
S0BG		FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Register	0000h
S0CON	**b**	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC	**b**	FF70h	D8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF		FEB2h	59	Serial Channel 0 Receive Buffer Register (read only)	XXXXh
S0RIC	**b**	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBUF		FEB0h	58h	Serial Channel 0 Transmit Buffer Register (write only)	0000h
S0TIC	**b**	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
S1BG		FEBCh	5Eh	Serial Channel 1 Baud Rate Generator Reload Register	0000h
S1CON	**b**	FFB8h	DCh	Serial Channel 1 Control Register	0000h
S1EIC	**b**	FF76h	BBh	Serial Channel 1 Error Interrupt Control Register	0000h
S1RBUF		FEBAh	5Dh	Serial Channel 1 Receive Buffer Register (read only)	XXXXh
S1RIC	**b**	FF74h	BAh	Serial Channel 1 Receive Interrupt Control Register	0000h
S1TBUF		FEB8h	5Ch	Serial Channel 1 Transmit Buffer Register (write only)	0000h
S1TIC	**b**	FF72h	B9h	Serial Channel 1 Transmit Interrupt Control Register	0000h
SP		FE12h	09h	CPU System Stack Pointer Register	FC00h

Special Function Registers Overview (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF0Ch	86h	CPU System Configuration Register	0XX0h*)
T0	FE50h	28h	CAPCOM Timer 0 Register	0000h
T01CON b	FF50h	A8h	CAPCOM Timer 0 and Timer 1 Control Register	0000h
T0IC b	FF9Ch	CEh	CAPCOM Timer 0 Interrupt Control Register	0000h
T0REL	FE54h	2Ah	CAPCOM Timer 0 Reload Register	0000h
T1	FE52h	29h	CAPCOM Timer 1 Register	0000h
T1IC b	FF9Eh	CFh	CAPCOM Timer 1 Interrupt Control Register	0000h
T1REL	FE56h	2Bh	CAPCOM Timer 1 Reload Register	0000h
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6	FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON	FFAEh	D7h	Watchdog Timer Control Register	0000h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

*) system configuration selected during reset

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 to + 70 °C
Storage temperature (T_{ST}) ..... – 65 to + 150 °C
Supply Voltage (V_{CC}) ..... + 6.5 V
Input voltage (V_{IN} min. = – 3.0 V for pulse width less than 15 ns) ..... – 0.5 to V_{CC} + 0.5 V
Power dissipation ..... tbd

Notes *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

The SAB 80C166 will also be offered in the temperature ranges – 40 to + 110 °C and – 40 to + 85 °C.

All of the following time specifications refer to a CPU clock of 20 MHz which is identical to an oscillator frequency (f_{OSC}) of 40 MHz.

DC Characteristics

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1	V	–
V_{IH}	Input High Voltage (all except RSTIN# and XTAL1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
V_{IH1}	Input High Voltage RSTIN#	0.6 V_{CC}	V_{CC} + 0.5	V	–
V_{IH2}	Input High Voltage XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	–
V_{OL}	Output Low Voltage (Ports 0, 1, 4, ALE, RD#, WR#, BHE#, CLKOUT, RSTOUT#)	–	0.4	V	I_{OL} = 2.4 mA
V_{OL1}	Output Low Voltage (all other outputs	–	0.4	V	I_{OL1} = 1.6 mA
V_{OH}	Output High Voltage Ports 0, 1, 4, ALE, RD#, WR#, BHE#, CLKOUT, RSTOUT#)	0.9 V_{CC} 2.4	–	V	I_{OH} = – 100 µA I_{OH} = – 2.4 mA
V_{OH1}	Output High Voltage (in all outputs)	0.9 V_{CC} 2.4	–	V V	I_{OH} = – 50 µA I_{OH} = – 1.6 mA
I_{OZ}	Input Leakage Current (Ports 0, 1, 2, 3, 4, NMI#, EBC0, EBC1)	–	±1	µA	0 V<V_{in}<V_{CC}

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
R_{RST}	Reset Pullup Resistor	50	150	kΩ	–
I_{IL}	XTAL1 Input Current	–	tbd	µA	$0 V < V_{in} < V_{CC}$
C_{IO}	Pin Capacitance (digital inputs/outputs)	–	10	pF	f = 1 MHz T_A = 25 °C
I_{CC}	Power Supply Current	–	180	mA	1/TCL = 40 MHz
I_{ID}	Idle Mode Supply Current	–	20	mA	1/TCL = 40 MHz
I_{PD}	Power Down Mode Supply Current	–	100	µA	V_{CC} = 2.5 V [1]

A/D Converter Characteristics

T_A = 0 to +70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 0.2 V; V_{AGND} = V_{SS} ± 0.2 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{AIN}	Analog Input Voltage	V_{SS} – 0.2	V_{CC} + 0.2	V	–
C_I	Analog Input Capacitance	–	70	pF	–
t_S	Sample Time	–	63 TCL		2)
t_C	Conversion Time	–	390 TCL		3)
TUE	Total Unadjusted Error	–	± 2	LSB	–
I_{REF}	V_{AREF} Supply Current	–	5	mA	4)
I_{AIN}	Analog Input Current	–	± 500	nA	5)

Notes

1) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{CC} – 0.1 V to V_{CC}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

2) This parameter specifies the time during which the input capacitance C_I can be charged/decharged by the external source. It must be guaranteed, that the input capacitance C_I is fully loaded within these 63 TCLs. 63 TCL is 1.575 µs at 20 MHz CPU clock. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time TS. 390 TCL is 9.75 µs at 20 MHz CPU clock.

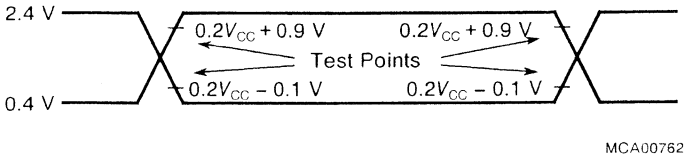
4) I_{REF} in Power Down Mode: TBD

5) This parameter specifies the static input current for an analog input channel, e. g. when the channel is not selected for conversion.

AC Characteristics

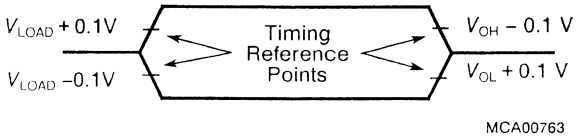
Testing Waveforms

Figure 8
Input Output Waveforms



AC Inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 9
Float Waveforms

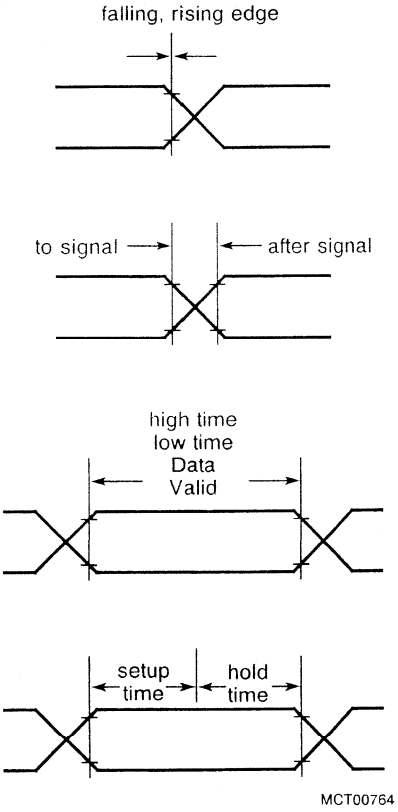


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

AC Characteristics (cont'd)

In the AC Characteristics waveforms, the mid-point of a signal transition is mostly used as the timing reference point. If not specifically specified in the drawings, the exact timing reference points are given by the parameter description according to the following figures (test voltage levels and float state references shown on previous page):

Figure 10
Timing Reference Points

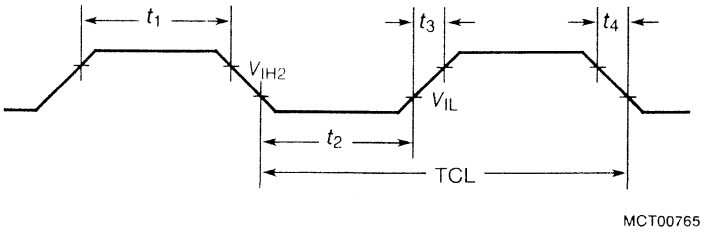


AC Characteristics (cont'd)

External Clock Drive XTAL1
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
TCL	Oscillator Period	25	25	25	500	ns
t_1	High Time	6	–	6	–	ns
t_2	Low Time	6	–	6	–	ns
t_3	Rise Time	–	5	–	5	ns
t_4	Fall Time	–	5	–	5	ns

Figure 10
External Clock Drive XTAL1



AC Characteristics (cont'd)

Multiplexed Bus with Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 6 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_7	Address Hold after ALE	15	–	TCL – 10	–	ns
t_8	ALE Falling Edge to RD#, WR#	15	–	TCL – 10	–	ns
t_{10}	Address Float after RD#, WR#	–	5	–	5	ns
t_{12}	RD#, WR# Low Time	40	–	2TCL – 10	–	ns
t_{14}	RD# to Valid Data In	–	35	–	2TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{19}	Data Float after RD#	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{23}	Data Hold after WR#	35	–	2TCL – 15	–	ns
t_{25}	ALE rising edge after RD#, WR#	35	–	2TCL – 15	–	ns
t_{27}	Address Hold after RD#, WR#	35	–	2TCL – 15	–	ns

Figure 11
External Memory Read Cycle

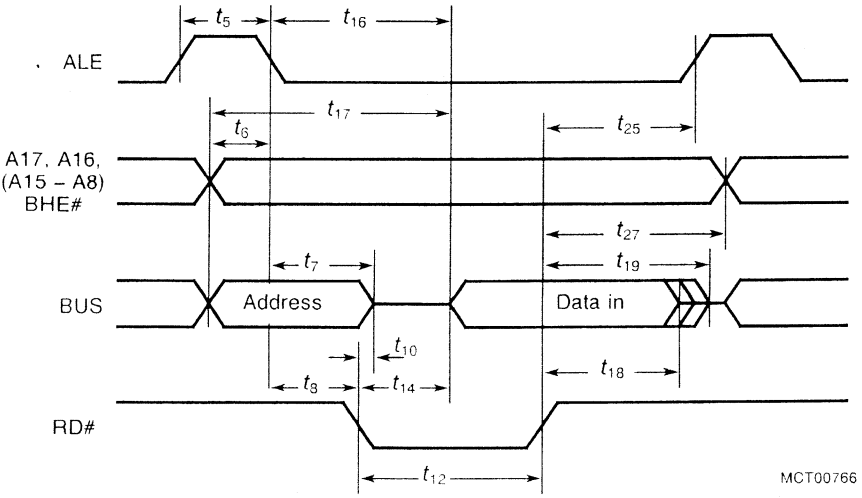
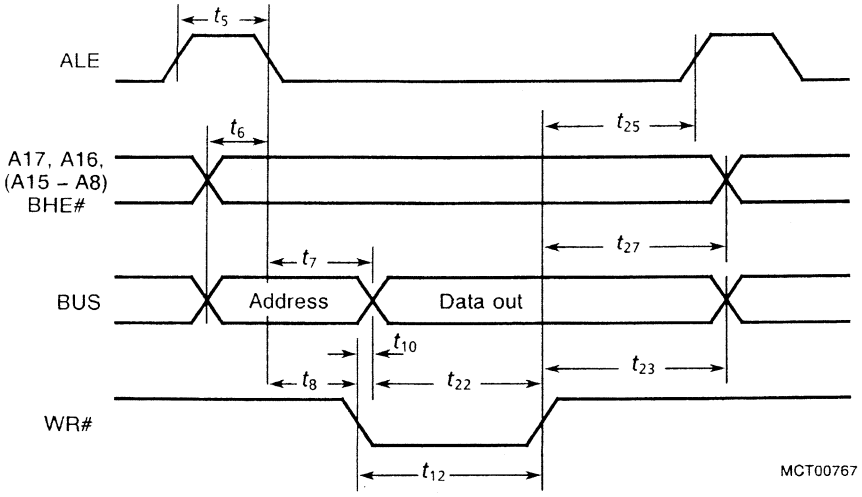


Figure 12
External Memory Write Cycle



AC Characteristics (cont'd)

Multiplexed Bus without Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 6 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_7	Address Hold after ALE	15	–	TCL – 10	–	ns
t_9	ALE Falling Edge to RD#, WR#	– 10	–	– 10	–	ns
t_{11}	Address Float after RD#, WR#	–	30	–	TCL + 5	ns
t_{13}	RD#, WR# Low Time	65	–	3TCL – 10	–	ns
t_{15}	RD# to Valid Data In	–	60	–	3TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{19}	Data Float after RD#	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{23}	Data Hold after WR#	35	–	2TCL – 15	–	ns
t_{25}	ALE rising edge after RD#, WR#	35	–	2TCL – 15	–	ns
t_{27}	Address Hold after RD#, WR#	35	–	2TCL – 15	–	ns

Figure 13
External Memory Read Cycle

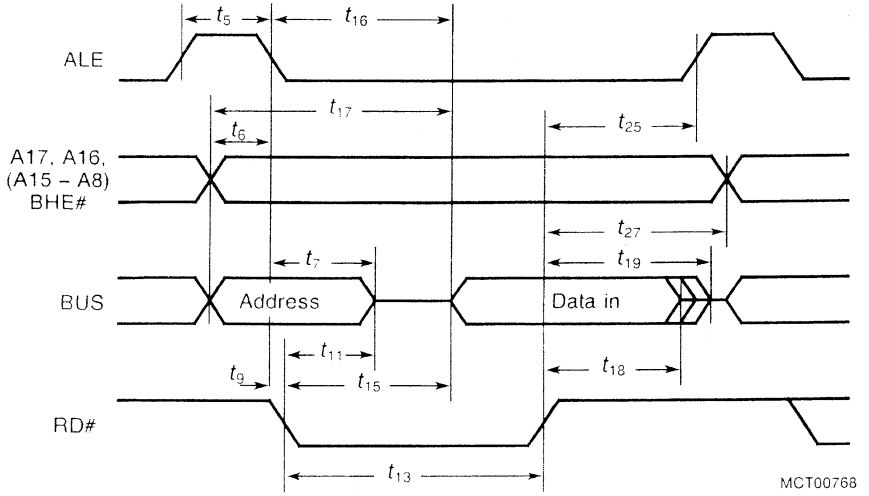
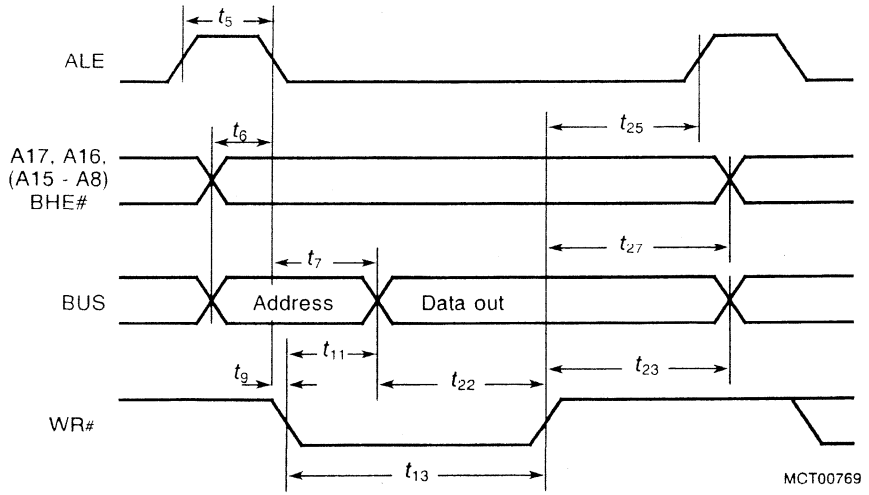


Figure 14
External Memory Write Cycle



AC Characteristics (cont'd)

Non-Multiplexed Bus with Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 4 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_8	ALE Falling Edge to RD#, WR#	15	–	TCL – 10	–	ns
t_{12}	RD#, WR# Low Time	40	–	2TCL – 10	–	ns
t_{14}	RD# to Valid Data In	–	35	–	2TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{20}	Data Float after RD# *)	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{24}	Data Hold after WR#	15	–	TCL – 10	–	ns
t_{26}	ALE rising edge after RD#, WR#	– 10	–	– 10	–	ns
t_{28}	Address Hold after RD#, WR#	0	–	0	–	ns

*) This time may be longer if no external bus conflict can occur. For example, this requirement is always met if only code but no data are accessed externally.

Figure 15
External Memory Read Cycle

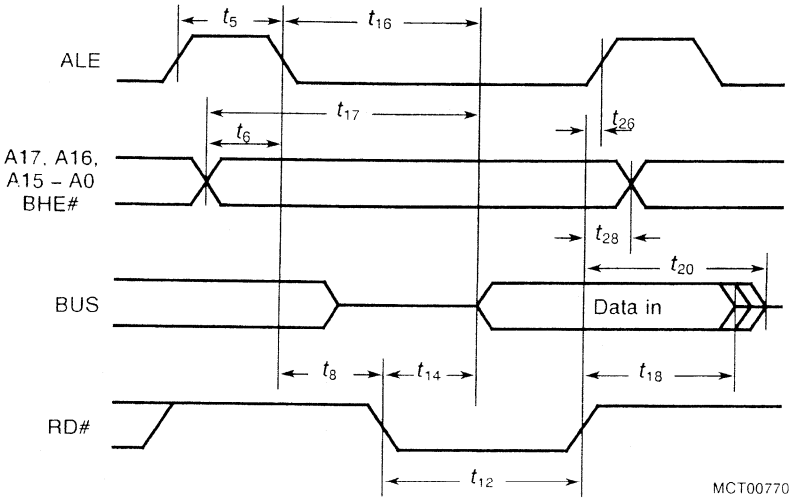
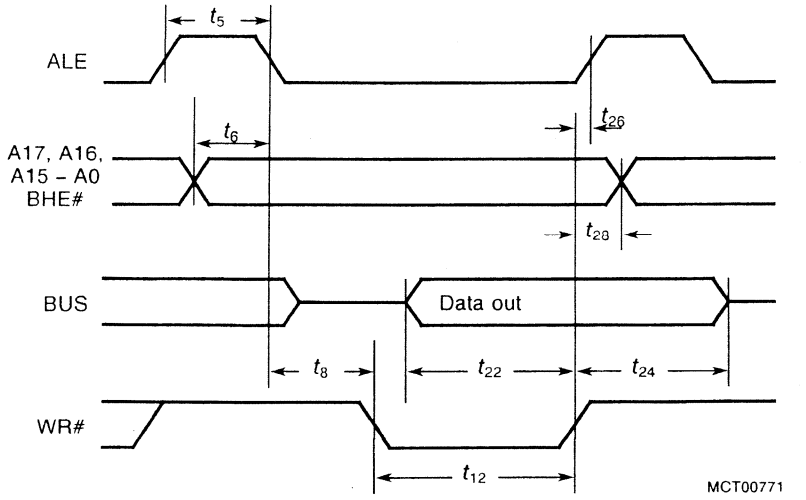


Figure 16
External Memory Write Cycle



AC Characteristics (cont'd)

Non-Multiplexed Bus without Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 4 TCL (100 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_9	ALE Falling Edge to RD#, WR#	– 10	–	– 10	–	ns
t_{13}	RD#, WR# Low Time	65	–	3TCL – 10	–	ns
t_{15}	RD# to Valid Data In	–	60	–	3TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{21}	Data Float after RD# *)	–	15	–	TCL – 10	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{24}	Data Hold after WR#	15	–	TCL – 10	–	ns
t_{26}	ALE rising edge after RD#, WR#	– 10	–	– 10	–	ns
t_{28}	Address Hold after RD#, WR#	0	–	0	–	ns

*) This time may be longer if no external bus conflict can occur. For example, this requirement is always met if only code but no data are accessed externally.

Figure 17
External Memory Read Cycle

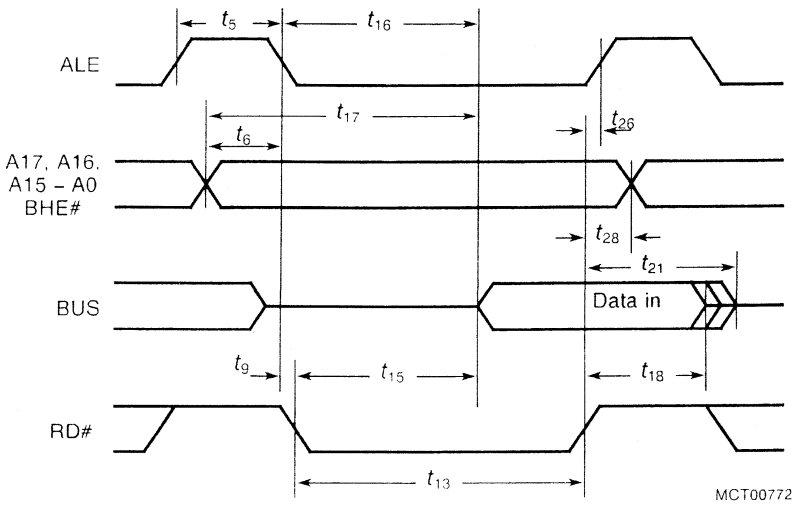
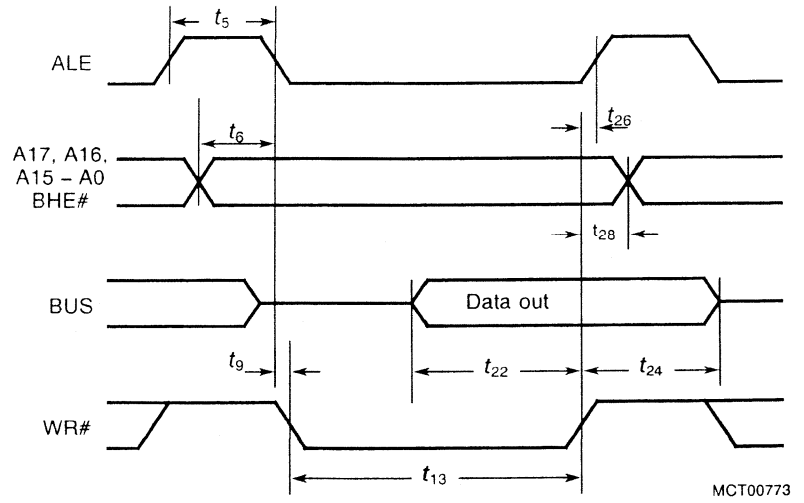


Figure 18
External Memory Write Cycle



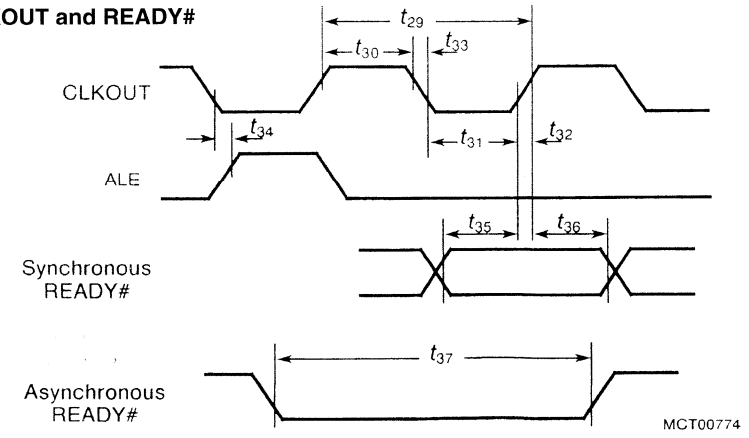
AC Characteristics (cont'd)

CLKOUT and READY#

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_{29}	CLKOUT Cycle Time	50	50	2TCL	2TCL	ns
t_{30}	CLKOUT High Time	15	–	TCL – 10	–	ns
t_{31}	CLKOUT Low Time	15	–	TCL – 10	–	ns
t_{32}	CLKOUT Rise Time	–	5	–	5	ns
t_{33}	CLKOUT Fall Time	–	5	–	5	ns
t_{34}	ALE Rising to CLKOUT Falling Edge	0	10	0	10	ns
t_{35}	Synchronous READY# Setup Time to CLKOUT	10	–	10	–	ns
t_{36}	Synchronous READY# Hold Time after CLKOUT	10	–	10		ns
t_{37}	Asynchronous READY# Hold Time	65	–	2TCL + 15	–	ns

Figure 19
CLKOUT and READY#



Application Notes

3-Phase Sine Wave Generation with the SAB 80C515A and SAB 80C517A
by Nikolaos Papadopoulos, Siemens AG - Semiconductor Division

Almost every industrial application needs the generation of analog output voltages with variable frequency and level. Since, most of the time, additional control or monitoring tasks have to be performed, the simplest solution would be to have a single microcontroller covering both needs. In this case, the analog signal is generated using digital pulse width modulation (PWM). The generation of a symmetrical sinusoidal 3-phase system is one specific application example for the generation of analog voltages. Interesting target applications for such a 3-phase sine wave are controlling asynchronous motors (ASM) or the realization of uninterruptable power supplies (UPS). In the following description, methods of how to use the microcontrollers SAB 80C515A and the SAB 80C517A for generating a symmetrical 3-phase system are shown.

Contents

38 Features of the SAB 80C515A and the SAB 80C517A

The microcontrollers SAB 80C515A and SAB 80C517A are derived from their basic versions SAB 80C515 and SAB 80C517, respectively. They are backward compatible and yet show inhanced or new features resulting in higher performance (see **figures 1 and 2**).

One speciality is the maximum clock input frequency (18 MHz) which means a 50% increase compared to the previous standard frequency of 12 MHz. The computational power of the SAB 80C517A is increased more than 10 times by the on-chip arithmetic co-processor. This Multiply/Divide Unit (MDU) executes multiply (16 × 16) and divide operations (32/16) as well as shift and normalize (32 bit) operations within 4 µsec. This facilitates floating point arithmetic, a fact that is especially important in high-level language programming (e.g. C).

The ROM versions SAB 83C515A-5 and SAB 83C517A-5 offer 32 KBytes on-chip program memory, allowing the engineer to expand it externally up to 64 KByte. Even higher address ranges can be achieved through bank switching which is supported by special linkers/locators. The ROMless versions SAB 80C515A and SAB 80C517A need external program (EP)ROM. Other than that, the ROM and the ROMless parts do not differ. In the following text, the numbering SAB 80C515A and SAB 80C517A also applies for the ROM parts (unless otherwise noted).

The on-chip data memory of the SAB 80C515A is expanded by an extra 1024 Bytes, whereas the SAB 80C517A incorporates an additional 2048 Bytes of internal data memory, compared to the 256 Bytes in the basic types. This sums up to 1280 Bytes and 2304 Bytes, respectively. Thus, in most applications an external RAM is obsolete which helps to minimize board space and cut down system cost.

Processing of analog signals is supported by the integrated A/D converter with genuine 10 bit resolution. The SAB 80C515A provides eight, the SAB 80C517A twelve multiplexed input channels. The total conversion time is less than 13 µsec, with the maximum total unadjusted error (TUE) being 2 LSBs. The ADC can be programmed to convert in single or continuous mode and can also be triggered externally.

For digital signal generation and measurement, the SAB 80C515A offers besides the two standard timers (T0/T1) the Timer 2 block which provides 4 capture/compare channels. In the SAB 80C517A, this Timer 2 block is located in the Capture/Compare Unit (CCU) which also features a fast Compare Timer and up to 21 high speed outputs.

Serial communication, for example with a host or other microcontrollers within a multiprocessor network, is performed by one (SAB 80C515A) or two (SAB 80C517A) serial channels. Separate baudrate timers for each channel allow flexible baudrate generation at almost any clock frequency.

The SAB 80C515A/80C517A are also designed to work in systems which require higher system reliability. Therefore, both a watchdog timer (WDT) and an oscillator watchdog (OWD) were implemented to increase system integrity. The WDT makes sure that the whole controller is reset if the software fails to clear it periodically after a software anomaly. The OWD in contrast, monitors the system clock. On detection of an oscillator failure (e.g. in the case of a broken crystal), it takes over and brings the controller into a reset state. It only releases the part after the clock has been recovered.

Finally, the system design engineer can chose between 4 power saving modes: slow-down mode, idle mode, software controlled power-down mode (SWPD) and the brandnew hardware controlled power-down mode (HWPD). One remarkable advantage of HWPD are that it can be invoked by

applying a low level voltage, and exited by applying a high level voltage at a specific pin. The second advantage is that while in HWPD all port pins are floating (tri-state) which avoids sourcing current to external circuitry and helps to save power.

39 How to Generate Analog Voltages Using PWM

39.1 General Aspects

With digital PWM, a variable analog voltage level is achieved through variation of the duty cycle within a fixed time interval (PWM period T_{PWM}, **figure 3**). Integration over the internal T_{PWM} (e.g. with a low-pass filter) leads to the average output voltage during T_{PWM}. Depending on the length of the duty cycle, the level of the average voltage is a value between the digital supply voltages of the microcontroller (V_{SS} and V_{CC}). Variation the duty cycle from one interval to the next results is a variation of the average voltage level during each time interval. Thus, it is possible to change the output voltage step by step from one interval to the next. Appropriate variation of the duty cycle also allows to step-wise generate a sinusoidal voltage (see **figure 4**). The sine wave values are stored in a table that is cyclically accessed. When the PWM intervals are short enough, and through filtering, a smooth sine wave can be produced. If the output voltage is not intended to vary between V_{SS} and V_{CC}, but needs to have a zero crossing, the DC voltage can be decoupled, e.g. with a serial capacitor.

The duty cycle t_D within T_{PWM} can be calculated using the sine wave value u(i):

$$t_D = T_{PWM}/2 + u(i) \times T_{PWM}/2$$

where – 1 <= u(i) <= + 1; 0 <=i<=N (number of sample points).

Generally, you have free choice for the length of the PWM interval. However, physics limit the selectable range for the longest and the shortest time value (lowest and highest PWM frequency f_{PWM}). The lowest frequency depends on the quality of the lowpass filter or on the filtering capabilities of the motor connected to the PWM output. An additional requirement is the fact that many applications require f_{PWM} to be supersonic (above the audible range). On the other hand, switching loss increases as the PWM frequency rises. From this point of view, engineers normally attempt to keep f_{PWM} as low as possible. In addition, power switches have a maximum switching frequency (e.g. approximately 30 kHz for IGBTs).

Both amplitude and frequency of the sine wave to be generated can be varied.

The peaks of the sine wave depend on how much the rising edge of the duty cycle of a sine wave deviates from the center of T_{PWM}. This means that the amplitude can be chosen to be between 0 V and $V_{CC}/2$. In the above mentioned formula for t_D, voltage value u(i) has to be exchanged with the new voltage value u'(i), which can be calculated as follows:

$$u'(i) = u(i) \times a,$$

where a is the desired amplitude factor, which can be chosen to be between 0% and 100%.

Variation of the sine wave frequency can be achieved in three different ways:

1. Variation of time interval T_{PWM}

The shorter T_{PWM}, the shorter the sine wave period, that is the higher the sine wave frequency.

2. Variation of the number of sample points N

Sample points are the voltage values that represent the sine wave. The higher the number of sample points (while T_{PWM} remains the same), the longer the sine wave period, i.e. the lower the sine wave frequency. At the same time the resolution of the sine wave is increased.

3. Variation of repetition factor Z

By repeating every sample point once or several times, the sine wave length doubles, triples etc. (see **figure 5**). Thus, the sine period can be varied without the need for more sample points (therefore saving memory space!). On the other hand, the smoothness of the sine wave becomes worse.

With these variation possibilities, the formula for the sine wave frequency is as follows:

$$f_{SIN} = 1/T_{SIN} = 1/(T_{PWM} \times N \times Z)$$

T_{PWM}: PWM interval
N: number of sample points
Z: repetition factor for each sample point.

39.2 How to Generate a 3-Phase System

Every symmetrical 3-phase system consists of three sinusoidal voltages which are phase shifted by 120° from each other. Since a sine wave can be represented by a table of N sample points (using PWM), one "run through the table" corresponds to one sine wave period. A phase shift of an electrical angle of 120° therefore corresponds to a table shift of N/3, a phase shift of 240° corresponds to a table shift of 2N/3. Usually, N should be chosen such that it can be divided by 6. Thus, not only the number of shifts can be devided by 3 (you need three phases), but also the zero crossing point is a sample point. This is useful, because this way only one half of the wave needs to be sampled and stored in the table.

Conclusion: One sinusoidal phase can be represented by one single table with N sample points. The other two shifted phases are represented by the same table, but with the starting sample point being shifted by N/3 and 2N/3, respectively.

40 Microcontroller Facilities for 3-Phase Generation

40.1 The Timer 2 in the SAB 80C515A and the SAB 80C517A

Figure 6 shows the principle diagram of the timer 2 (T2) block. The maximum input clock of this 16-bit wide, free running timer is 1/12 of the oscillator frequency. This corresponds to a time increment of 667 nsec at 18 MHz. A programmable prescaler can divide the input frequency by 2 in the SAB 80C515A, which results in a maximum input frequency of $f_{OSC}/24$. The SAB 80C517A additionally allows the input frequency to be programmed to $f_{OSC}/48$ or $f_{OSC}/96$. In reload mode, the overflow time of timer 2 is programmable. An interrupt is flagged after every T2 overflow.

Timer 2 works with 4 (SAB 80C515A) or 5 (SAB 80C517A) capture/compare registers (CCx, x = 0 ... 3 or 4). Each of them is also 16-bits wide and controls one specific port pin (see **figure 6**). These capture/compare registers can be programmed to have one of three functions:

1. Capture function
Upon a rising edge at the corresponding port pin, CCx captures the current T2 contents and flags an interrupt. Thus, the moment when the signal edge occurred can be measured very accurately.

2. Compare function
Upon a match of T2 and CCx, a compare event at the corresponding port pin is generated and an interrupt is flagged. The compare function is subdivided in 2 different modes:

2a) Compare mode 0 (PMW mode)
Upon timer 2 overflow a LOW level appears at the corresponding compare output pin. Whenever the contents of T2 and CCx match, a HIGH level is output at the corresponding pin (**figure 7**).

2b) Compare mode 1
In this mode, the output pin is physically disconnected from the internal port latch. Every write access to the corresponding latch does not affect the pin immediately. Only after a compare match of T2 and CCx the value written to the latch appears at the pin. An overflow of timer 2 does not have any effects on the output pin.

3. Reload function
Register CC0 (also referred to as CRC, compare/reload/capture) can also be programmed to work as a reload register for T2. This means that after an overflow from FFFFH timer 2 does not re-start at 0000H, but at the value stored in register CRC.

For sine wave generation, the PWM mode is relevant (compare mode 0). The falling edge at the pin after every T2 overflow characterizes the interval T_{PWM}. It can be varied by operating timer 2 in auto-reload mode. The value in the reload register CRC determines the overflow time of T2 and thus T_{PWM}. The rising edge which determines the duty cycle, can be selected by loading the compare register with the appropriate value.

Both a compare match and a timer overflow set their own interrupt flags. After every compare match, the software has to take care that the compare interrupt is disabled for the rest of the T_{PWM}. The reason is that after every match the compare value for the next PWM period has to be loaded into CCx. However, it must be insured that this new value does not cause another compare match in the current interval. This would be the case, if the new value (for the next timer cycle) is higher than the previous one (that just caused the compare match), and the timer is yet to reach this value in the current cycle. It is not so much that this would affect the level at the pin (it is outputting a HIGH level anyway), but it would flag another interrupt. In this case, yet the next compare value would be

loaded into CCx without the current one causing the new interrupt (meant for the next timer cycle) having contributed to the PWM generation. Therefore, the compare interrupt should be disabled once it has been processed in a timer cycle. The timer overflow interrupt routine has to again enable the compare interrupt, of course only after having cleared the request flag that might have been set in the previous timer cycle.

40.2 The Compare Timer in the SAB 80C517A

The Compare/Capture Unit (CCU, see **figure 8**) of the SAB 80C517A contains besides the timer 2, a second 16-bit wide free running "compare timer" (CT). Up to 8 new compare registers (CM0 ... CM7) can be assigned to the CT, each of which have their dedicated output pins (alternative functions of port 4). The compare timer and the compare registers have been implemented especially to support PWM generation and therefore show some extraordinary features.
The maximum input clock for the compare timer is $f_{OSC}/2$. Thus, the increment time is 111 nsec (at f_{OSC} = 18 MHz). The input frequency can also be reduced by a 3-bit prescaler down to 1/256 of the oscillator frequency. The CT has its own auto-reload register CTREL which determines the overflow time and thus the PWM period T_{PWM}.

An example shows how the fast CT can be used for PWM generation. At 9-bit resolution (CTREL = FE00H) the switching frequency f_{PWM} is:

$f_{PWM} = 1/T_{PWM} =$
$= 1 / [(10000H - FE00H) \times 111 \text{ nsec}] =$
$= 1 / (512 \times 111 \text{ nsec}) = 17.6 \text{ kHz}.$

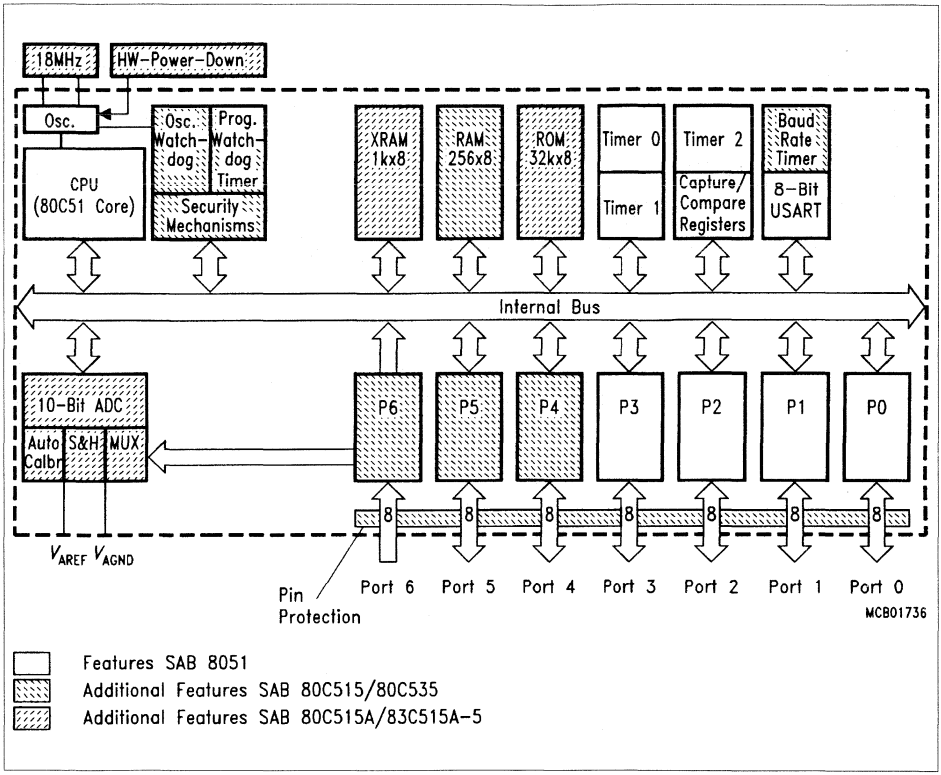
A very important characteristic of the compare registers CM0 ... CM7 is their double register structure together with the timer overflow control loading (TOC, see **figure 9**). The double register structure implies that the real register, which is constantly compared with the timer, is not accessible for the CPU. Whenever the CPU tries to write to one of the CMx registers via the internal bus, it instead accesses a shadow register. Its contents is only loaded to the actual compare register upon the CT overflow. This feature avoids the need to disable a compare interrupt and to re-enable it after the timer overflow (see chapter 4.2.4, "Generating the PWM Signals"). Thus, compare interrupts for PWM generation with registers CM0 ... CM7 are unnecessary and therefore not available.

41 Software Examples for 3-Phase Sine Wave Generation

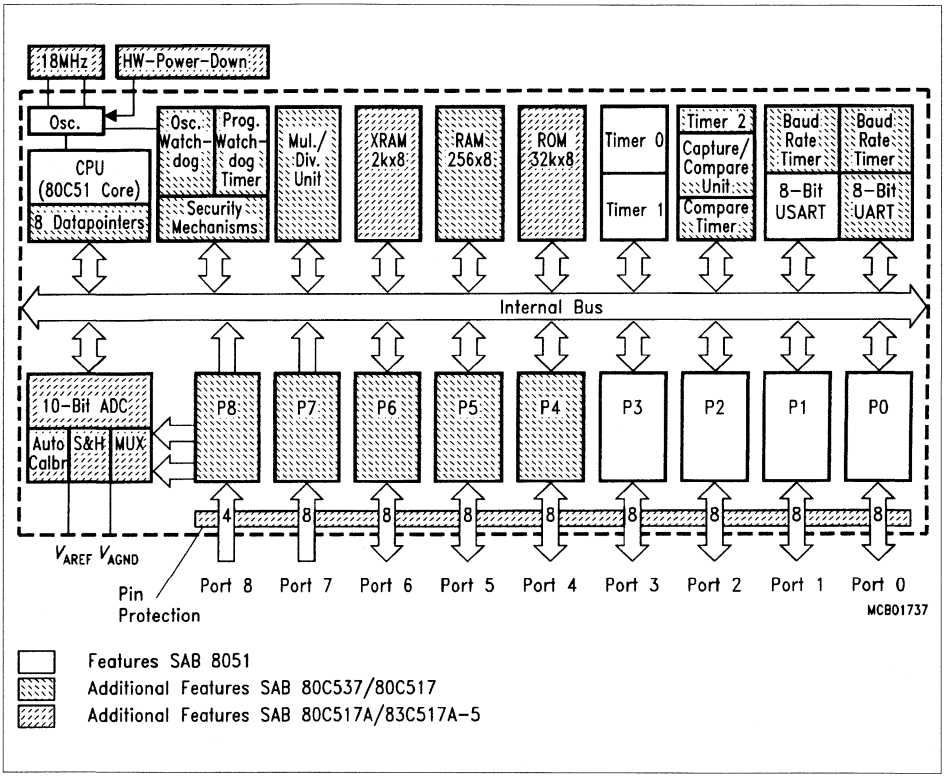
41.1 General Aspects

The two application examples that are presented in the following sections, show one possible realization of a 3-phase sine wave.

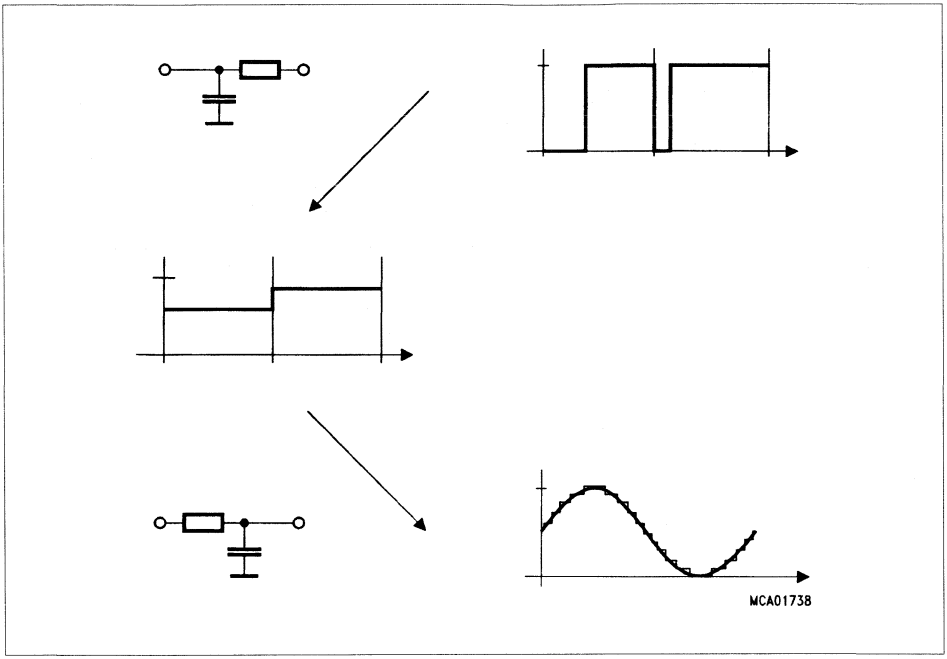
Annex A
Figures



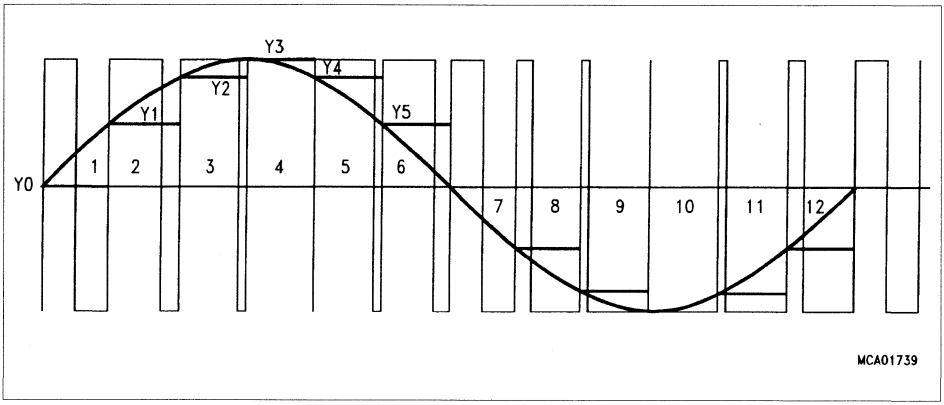
SAB 80C515A: Block Diagram



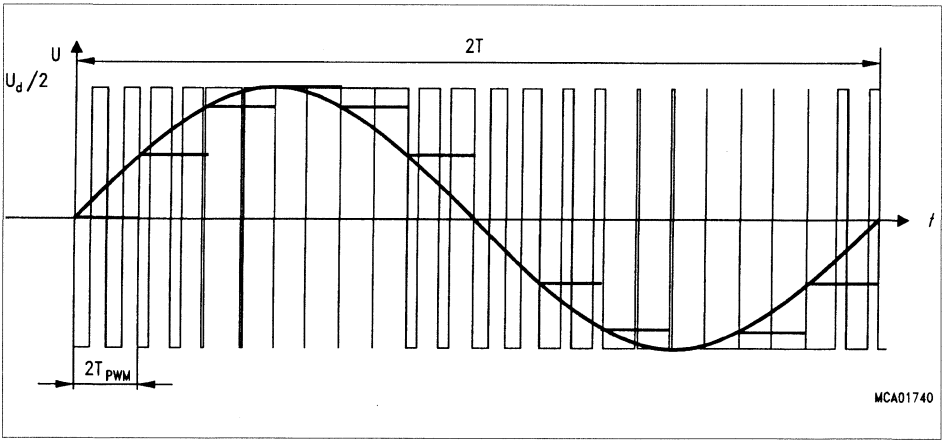
SAB 80C517A: Block Diagram



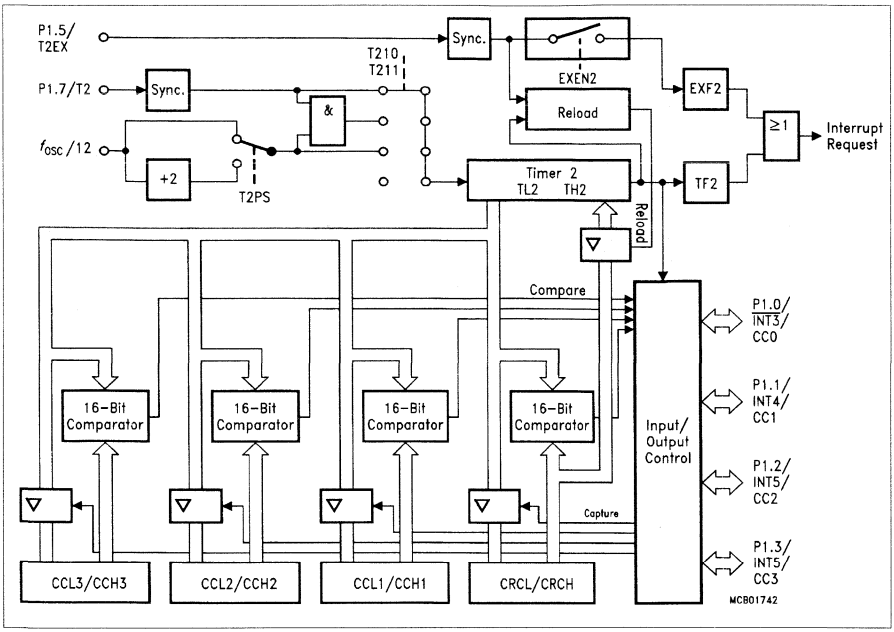
PWM Principle



Sine Wave Generation

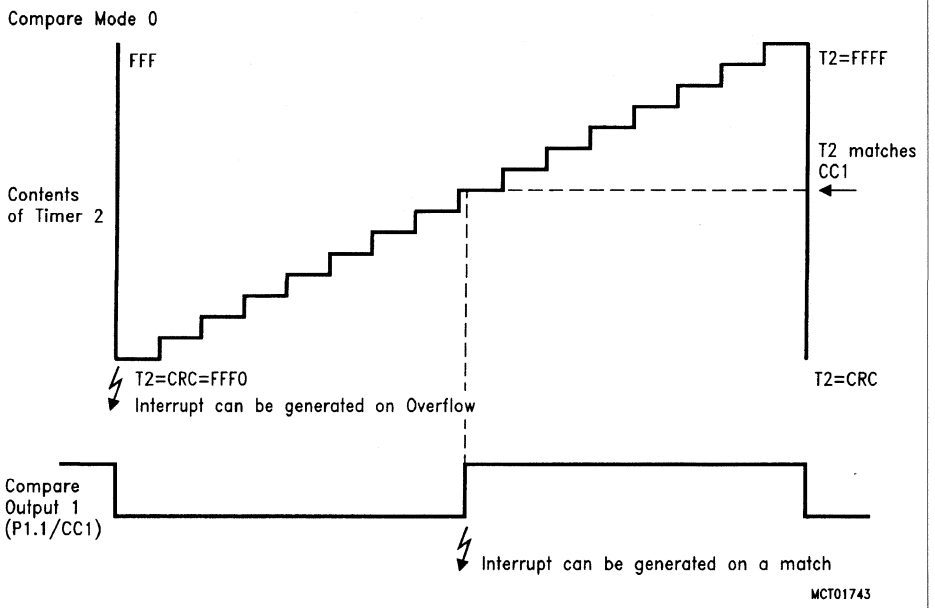


Doubling the Sine Frequency

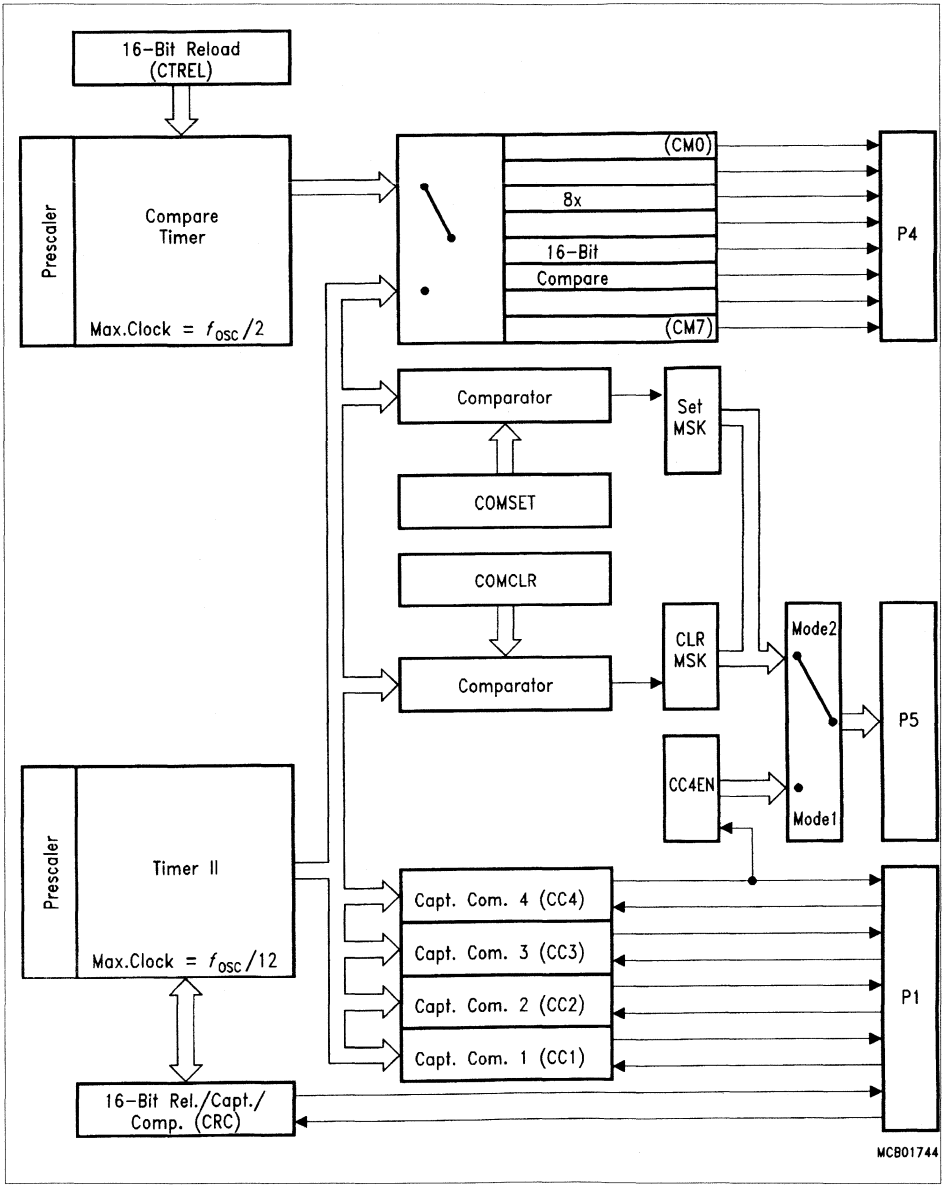


Timer 2 Block

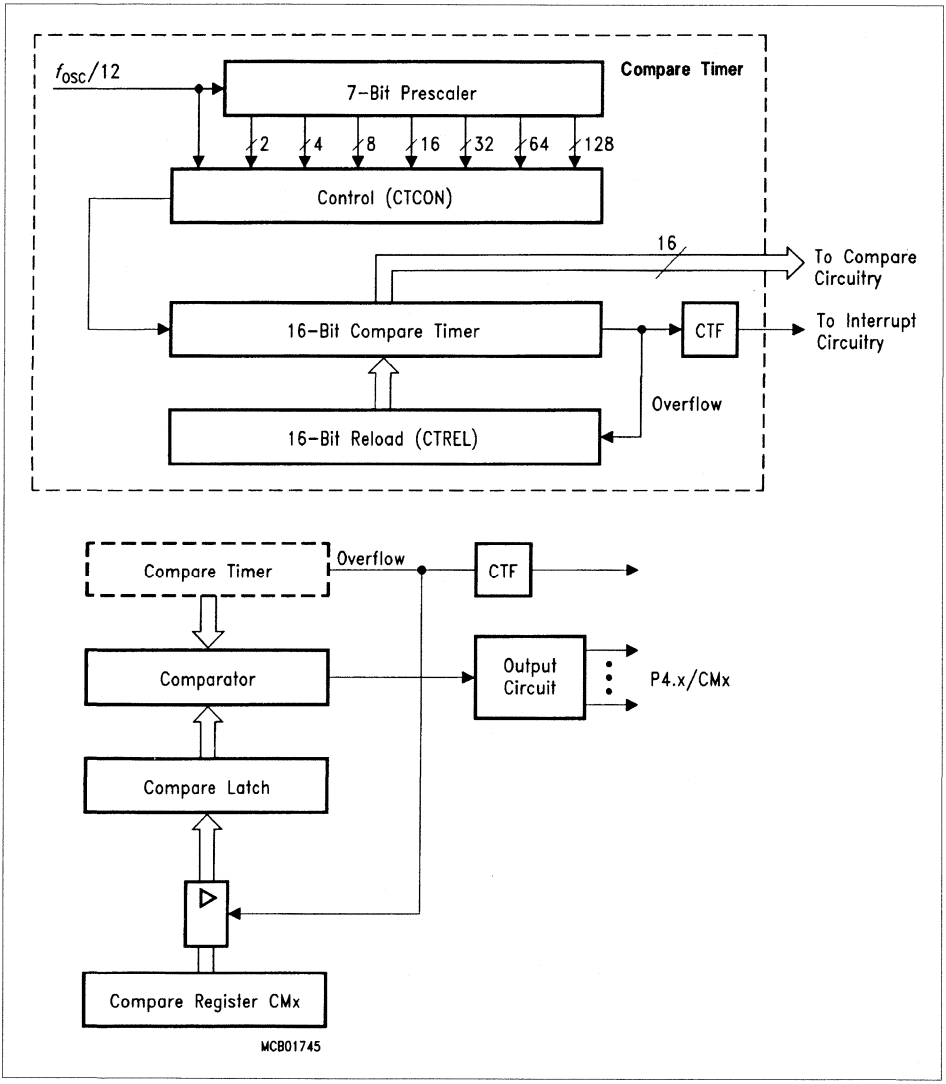
How to generate a PWM-signal with the SAB 80515 (e.g. PWM Period with 4 bit resolution):



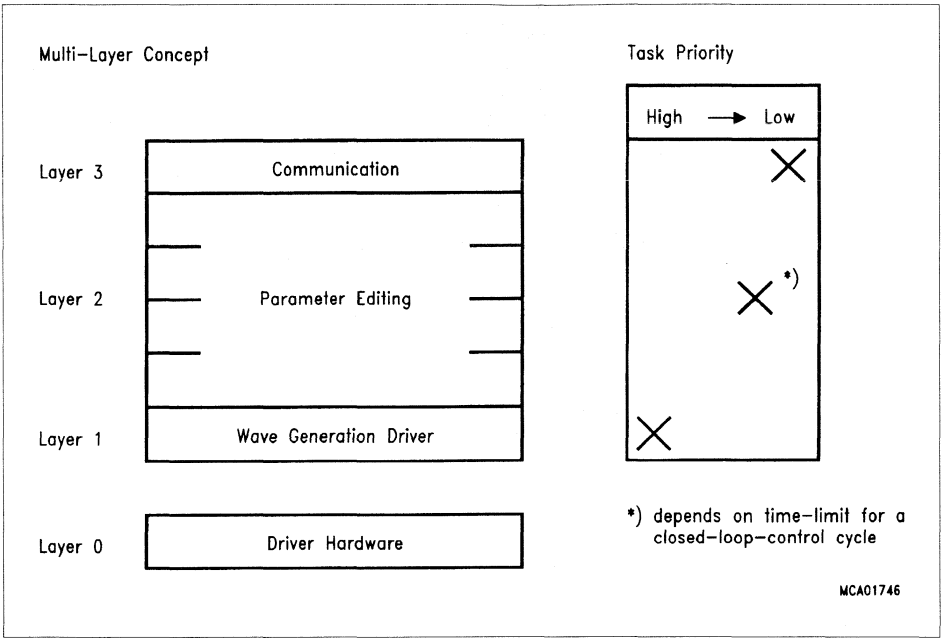
Compare Mode 0 (PWM Mode)



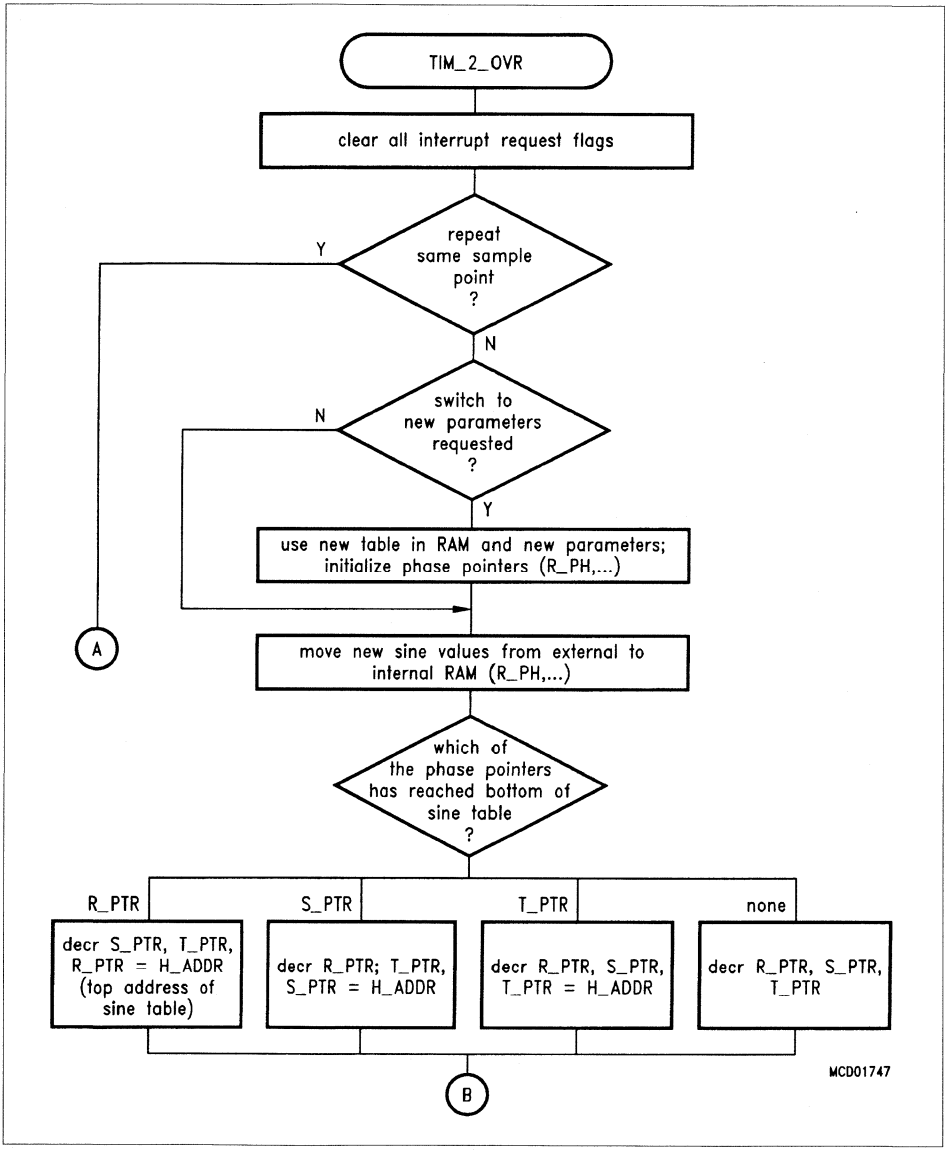
Compare Capture Unit (C517A)



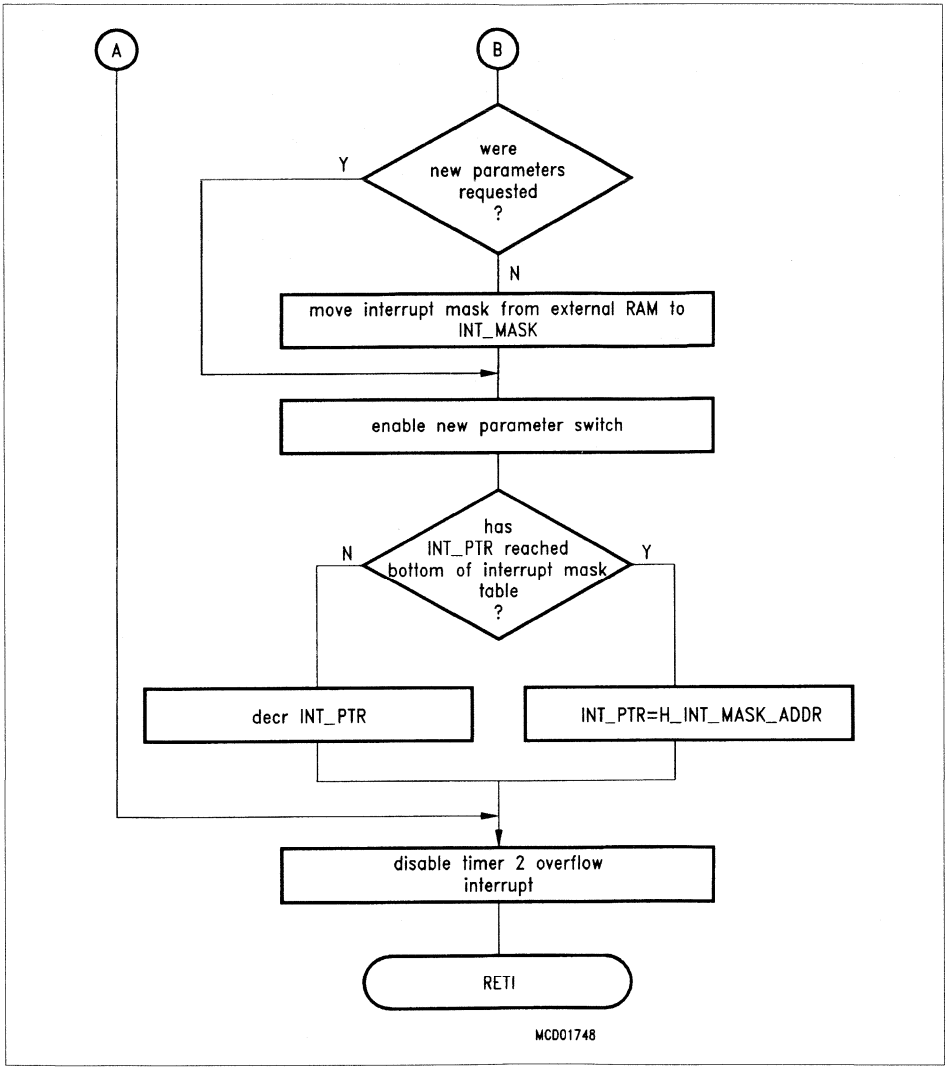
Double Register Structure CMx



Task Layers for Application Example

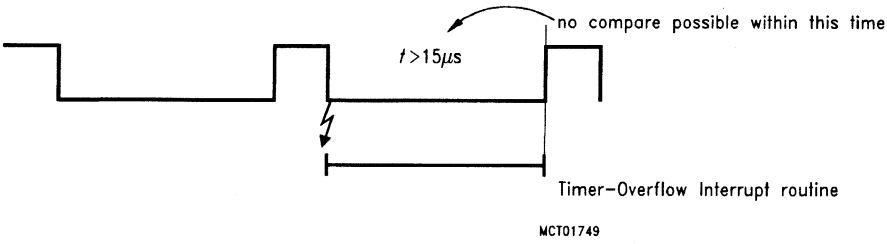


Flow Chart Timer 2 Interrupt (a)

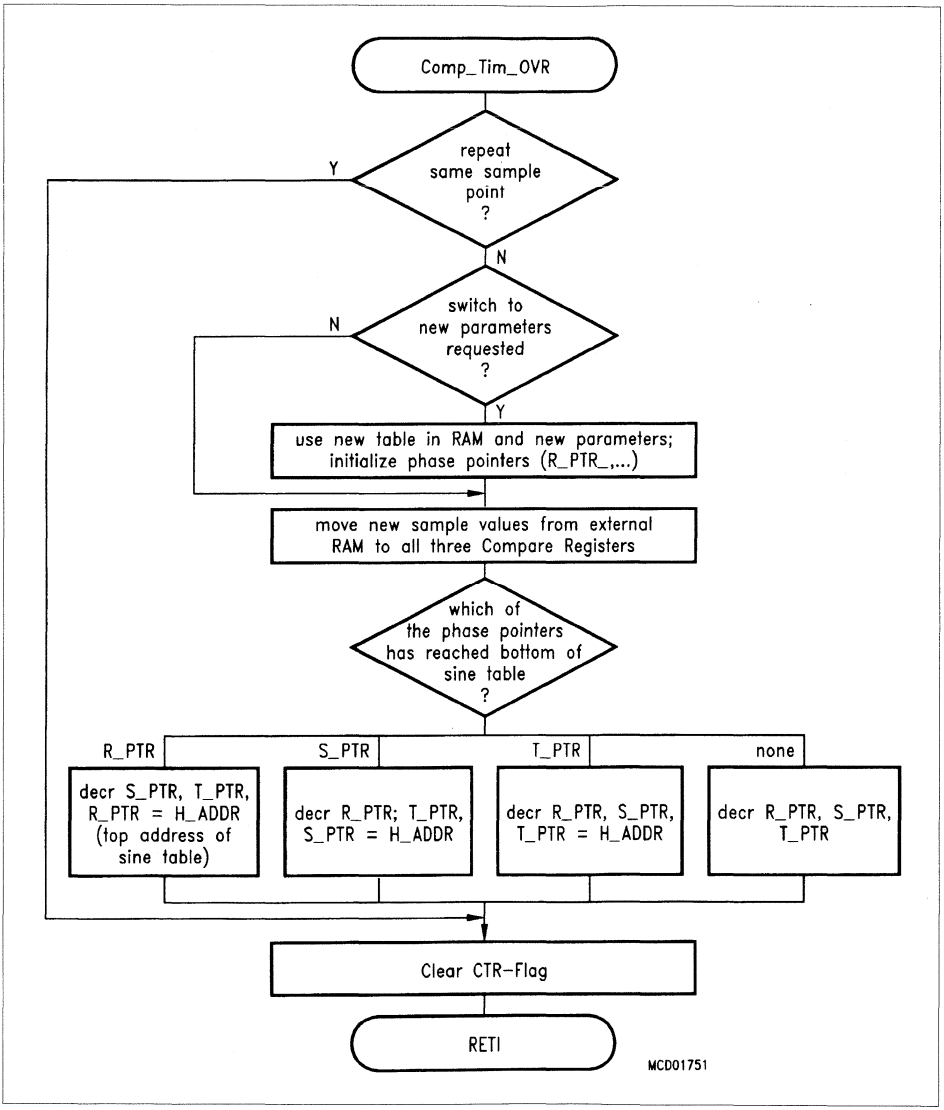


Flow Chart Timer 2 Interrupt (b)

Why „Interrupt Source Passing"?
Two proposals to think of a better way to generate a 3-Ph-PWM:
„Bad" Solution No. 1 Easiest and least time consuming way for the controller: use timer-overflow interrupt to load PWM-values for all three phases. Problem: Interrupt routine restricts minimal possible duty cycle.



Compare Reload: Bad Solution



Flow Chart Compare Timer Int.

B. Lienhard, HL MCB PM MC 2 / 07.06.1991 / Rel. 1.1

Application Note
Data Saving With The SAB 80C517A In Power Down

In industrial and automotive fields, there is a strong need to save system information or data even while the main power supply is switched off. This information could be setup data, configuration data, error messages or other important data which must be available once the system restarts its normal operation.

There are basically two different methods to meet this demand. In method number one, data saving is achieved using "none-volatile" storage media, such as EEPROMs. This solution can make board designs rather uneconomical, due to the high price of such devices. Thus, this solution is normally used when a long data saving time is required or when there is no other alternative to buffer data. In this case the two above mentioned facts have a higher priority than the price level. The second solution is used more often. It is based on buffering the information with a weak standby supply which preserves the data after the main power supply is switched off.

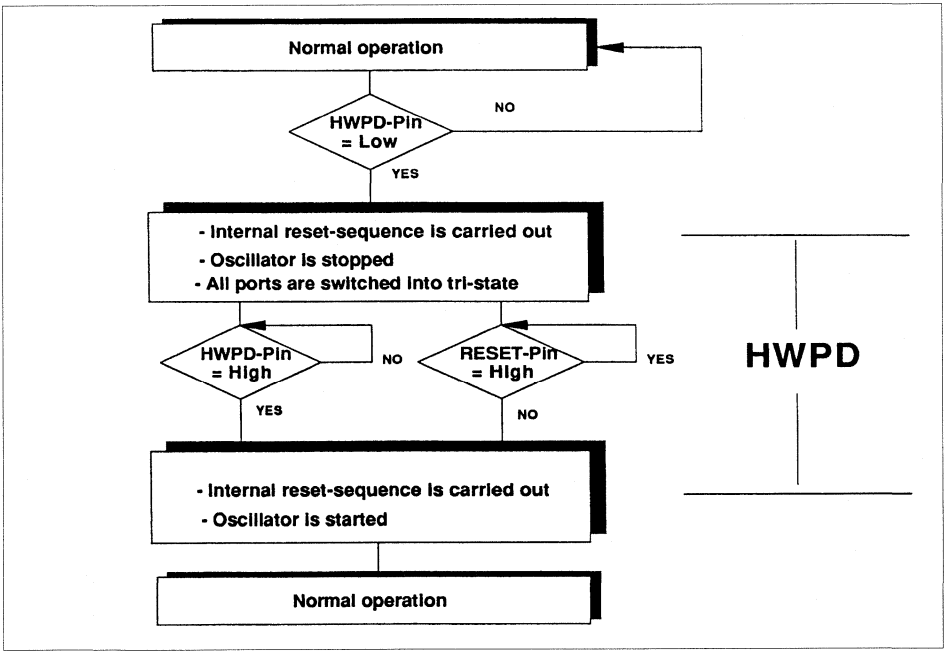
With the growing availability of larger on-chip RAM on microcontrollers (SAB 80C515A with 1280-bytes, SAB 80C517A with 2304-bytes) this second way of data saving is becoming more and more economical for most board designs. The two following application examples therefore show two different ways of saving important data in the internal RAM of the SIEMENS line of high end 8-bit microcontrollers.

The SAB 80C517A and its power down modes

The heart of these two application examples is the microcontroller SAB 80C517A. Before going into the details of the first application example this paragraph gives a short technical overview of the SAB 80C517A.

It is an 8-bit microcontroller with powerful peripheral components such as Multiplication and Division Unit (MDU), Capture/Compare Unit, real 10-bit Analog Digital Converter (ADC), two Serial Interfaces, 68 I/O-lines, 2304-byte internal RAM, fail safe mechanisms and, last but not least, four power down modes. The latter are of particular significance to these application examples. During normal operation the SAB 80C517A needs a supply current of lower than 28 mA (f_{osz} = 12 MHz). The power down modes are used to reduce this consumption. In each of these modes the content of the internal RAM (2304-bytes) is preserved. The SAB 80C517A has in total four different types of power down modes, the Idle-mode (IDM), the Slow-down-mode (SDM), the Software-power-down (SWPD) and the Hardware-power-down (HWPD). The Idle-mode, Slow-down mode and the Software-power-down are software initiated. In the Idle-mode only the CPU is stopped, while all peripheral components are still running. The ports retains their states. In the Slow-down-mode the controller runs with a reduced speed (1/8 oscillator frequency). The last of the software initiated power down modes is the Software-power-down. In this mode not only the CPU is stopped, as in the Idle mode, but also the on-chip peripherals are also stopped. During the SWPD the supply current is reduced, but the ports keep their last states active (can be inputs or outputs). This fact makes estimation of the power consumption rather difficult because the port loads influence this value. For example, some of the port lines are defined as outputs before entering the SWPD, these lines are still output lines during the Software-power-down. In this configuration the port loads take their required current from the controller. The supply current therefore increases.

The Hardware-power-down is a power down mode is initiated by an external hardware signal. For this mode the SAB 80C517A has one special input pin HWPD# (# = low active). A low signal at the HWPD# pin stops the running software and carries out the internal power down sequence (**figure 1**). During this mode the SAB 80C517A is completely disconnected from its periphery as all ports are in tri-state. As it is independent of any port loads this unique feature guarantees a supply current below 50 µA.

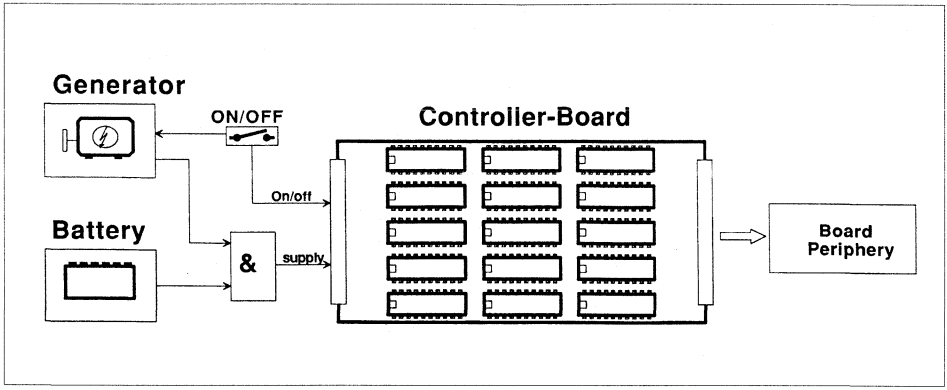


How to enter and leave the HWPD in the SAB 80C517A

To detect the power down request the microcontroller scans the level of the HWPD# pin in every machine cycle. If this pin is low, the internal power down sequence is executed. This sequence starts with a normal reset phase, then the internal oscillator is stopped and all ports are switched into tri-state. Now the SAB 80C517A is in power down. There are two ways of "waking up" the controller. The first is to set the HWPD# pin to logical high; the second is to reset the SAB 80C517A. Futhermore, the reset has a higher priority than the HWPD. In both cases the controller starts working with a normal reset sequence. Due to the internal oscillator watchdog of the SAB 80C517A this restart lasts less than 18 µs. After this restart the controller runs the implemented software.

Application No. 1 - SAB 80C517A with the SIEMENS voltage regulator TLE 4258

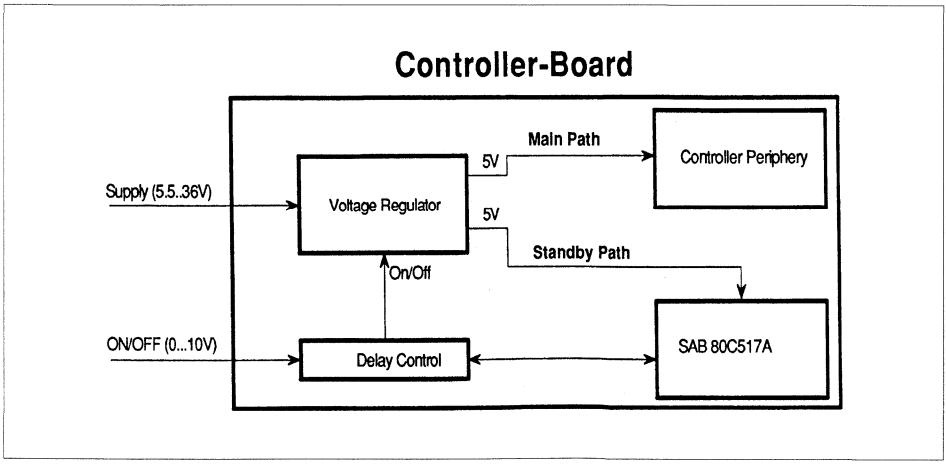
Description of the system environment. (**Figure 2**)



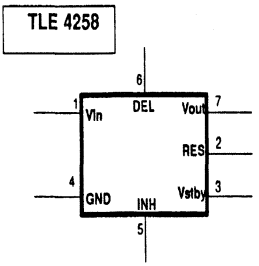
The controller-board is supplied from two external sources (generator and battery). During normal operation the generator is turned on and supplies the controller board. In the standby mode the generator is switched off and the battery serves the controller board. Additionally, the status line indicates the operation change.

To guarantee a long life span for the battery the most important point is to reduce the power consumption of the controller board to a minimum (automotive systems for example allow a maximum standby current of 1 mA for the whole board).

In figure 3 the structure of the controller board is demonstrated.

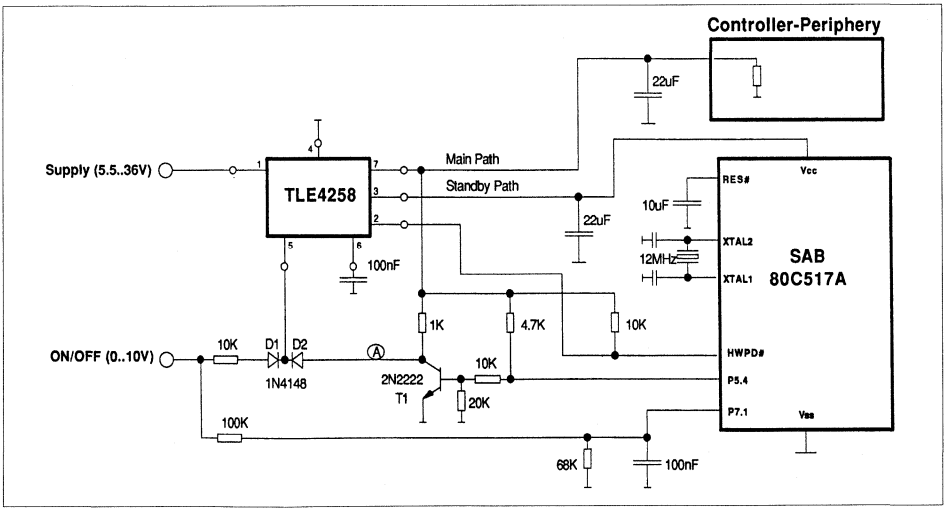


Due to the above mentioned requirement to reduce the power consumption to a minimum, the complete controller periphery must be switched off, while the SAB 80C517A must still be supplied with 5 V. The easiest way to achieve this is to use a voltage regulator with two separate output paths (main path, standby path). The main path (which can be switched on and off) is used to support the controller's periphery, while the standby path serves only the SAB 80C517A in both operation modes (normal operation, power down mode). In this application example the SIEMENS low drop voltage regulator TLE 4258 is used (**figure 4**).



Vin (pin 1):	Input voltage 5.5V..36V
Res (pin 2):	Reset pin (low active)
Vstby (pin 3):	Standby path, Imax 35mA
GND (pin 4):	Ground
INH (pin 5):	Switch on/off (Vinh >3.6V --> switch on, Vinh < 3.6V --> off)
DEL (pin 6):	Delay time for reset
Vout (pin 7):	Main path, Vout = 5V +/- 15%, Imax = 300mA

The SAB 80C517A is directly supplied by the standby path of the TLE 4258. The maximum current at this path is determined by the microcontroller in normal operation mode. This current is lower than 28 mA, if the SAB 80C517A is clocked with 12 MHz (**figure 5**). In HWPD mode this current is reduced below 50 µA. The HWPD# pin is connected to the reset pin of the TLE 4258, so an active reset signal (even in case of undervoltage!) of the voltage regulator causes the SAB 80C517A to go into Hardware-power-down mode.



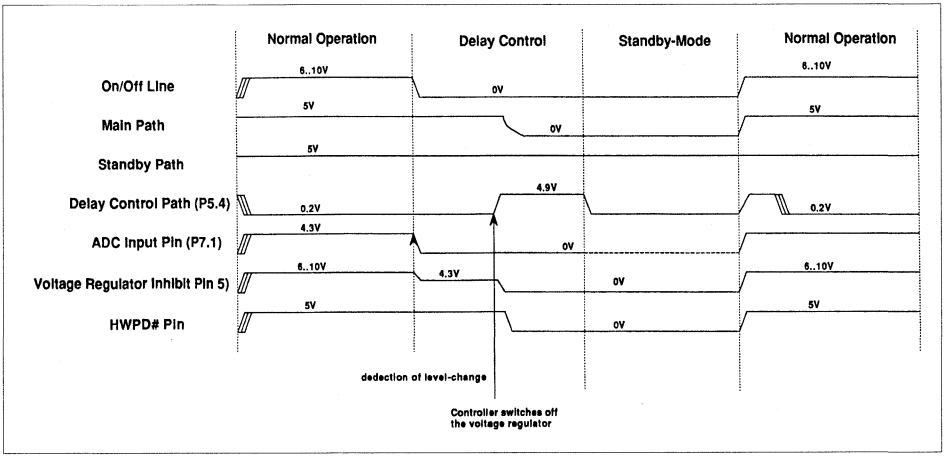
As already explained, the main intention is to save important data in the internal RAM of the SAB 80C517A when the system is in standby mode. These data can be status/setup information, error messages or other important system data. In order to write these data into the internal RAM the controller must know when there is an external requirement for the controller board to switch into standby mode. For that purpose the status line is connected through one of the analog input pins (P7.1) to the internal Analog Digital Converter (ADC).

The connection is carried out with two resistors and a capacitor to reduce the input voltage to 4 V. The capacitor together with the 100 K resistor works like a low-pass to avoid spikes at the ADC input pin. This, and the two internal clamping diodes, protect the analog input pin against damage. The software uses the internal ADC to monitor the status line. If its level is 4 V the status line indicates that normal operation is to be continued. If it is well below 4 V the controller recognizes that it should switch to standby mode. In this case there is no current flowing through the diode D1. Therefore, the state of the voltage regulator noe depends solely on the state of the transistor T1. The circuit layout in figure 5 shows, that this transistor is controlled by the pin P5.4. If the controller outputs a low at this pin the transistor T1 is turned off. The voltage level is therefore 5 V at point A. Consequently the regulator is consequently still active. This control of the voltage regulator through diode D2 is called delay control. Delay control is required if the internal RAM of the SAB 80C517A does not contain the latest data when the status line becomes active. In this case the controller starts the updating sequence (e.g. reading data from external peripherals). After this is finished the SAB 80C517A turns off the regulator by outputting a high at P5.4. As a consequence the voltage of the main path drops down from 5 V to 0 V. The reset pin of the voltage regulator becomes active and pulls the HWPD# pin low as well. The voltage at the standby path is still at 5 V and provides the power down current for the SAB 80C517A.

How to switch on the regulator

When the external generator starts working again, the status line becomes active and switches on the voltage regulator through diode D1. The voltage on the main path is then 5 V again. This causes the reset pin of the TLE 4258 to become inactive. This level change will release the controller from hardware power down, because there is now a logical high at the HWPD# pin. After executing the internal reset sequence, the SAB 80C517A starts working. At the beginning of this startup the port pin P5.4 must be cleared to activate the delay control.

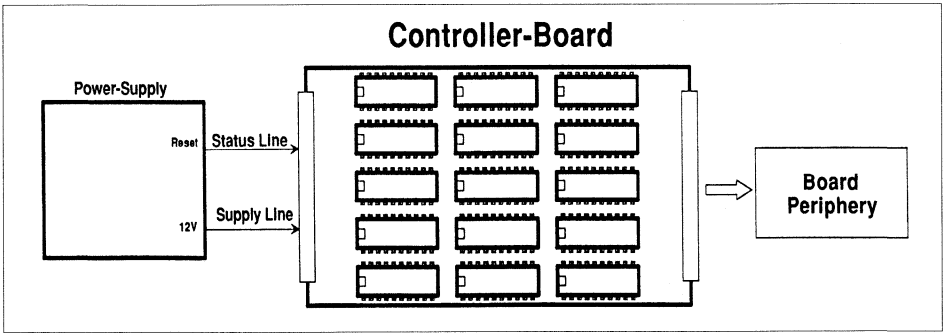
The figure 6 shows the context of these signal timing of the various pins.



The corresponding software example is given in figure 10.

Application No. 2 - The SAB 80C517A in combination with the SIEMENS voltage regulator TLE 4261

The application example No. 1 describes a system configuration with two supply sources (main power supply, standby supply) situated outside of the controller board. The supply switch between normal operation and standby was also realized outside the board. In application example No. 2 another method of data saving, with two separate supplies, is demonstrated.



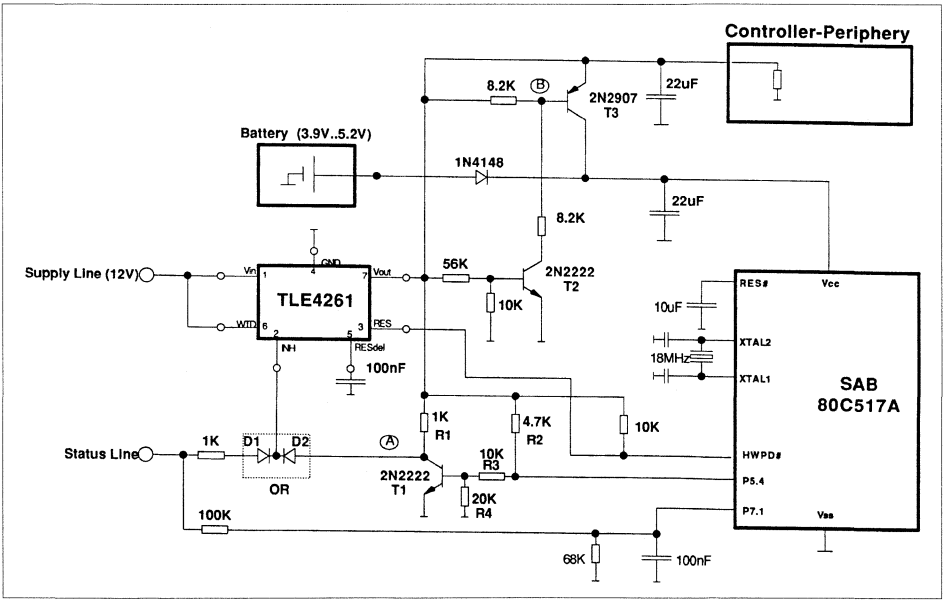
Before dealing with the details of the circuit layout, a brief description of the system environment illustrated in figure 7.

In normal operation mode the controller board is served by a main power supply via a supply line. This power supply outputs 12 V. If this supply is turned off it is indicated by a status line. As a consequence the status line becomes active (low active) and forces the controller board to go into standby mode.

How the controller board manages the status/supply line

The core of this controller board is, as in the previous application example, the 8-bit microcontroller SAB 80C517A. The large on-chip RAM of this controller is used to buffer important data during standby mode. As the main power supply is switched off in standby mode, there must be another source to provide the controller's standby current. This standby source a battery - for example - is located on the controller board.

The supply line from the main power supply is connected with the input pin (pin 1) of the voltage regulator TLE 4261. As mentioned above, this line has 12 V.



In this controller board design the TLE 4261 is used to convert the 12 V from the main power supply into 5 V for the board. The TLE is a low drop voltage regulator with just one output path providing 5 V +/– 5%. In the standby mode this regulator is switched off and only the SAB 80C517A is then supported by the battery. During this standby mode the controller is in Hardware-power-down (power consumption falls below 50 µA) and the content of the internal RAM is saved. When the main power supply is turned on again the status line goes to high and switches on the voltage regulator as well.

Description of the circuit layout

As in application example No. 1 control of the voltage regulator is achieved by a delay control. This is also used in application example No. 2 and consists of the transistor T1, the corresponding resistors R1, R2, R3 and R4, the two diodes D1, D2 and represents a cost efficient solution for the control of the voltage regulator. The two diodes representing an OR connection. The output of this OR serves the INH pin of the TLE 4261 (regulator on/off) and depends on the state of the transistor T1 and the status line. In normal operation the status line is approximately 10 V. This results in a voltage level of 9.3 V at the INH pin. In this case the TLE 4261 is active and outputs 5 V at pin 7. To active the delay control, the SAB 80C517A clears the port pin P5.4. This turns off the transistor T1 and pulls the voltage level at point A to 5 V. To monitor the status line and to detect whether there is any intention to switch off the main power supply, the internal 10 bit ADC of the SAB 80C517A is used. The status line is connected to one of the twelve analog input channels.

This connection is realized via two resistors (100 K, 68 K) and a capacitor (100 nF). This kind of input protection reduces the voltage of the status line to 4 V and avoids spikes at the ADC input pin (low-pass). Used in conjunction with the internal clamping diodes, this ensures that the analog input pin is well protected against damage.

When the status line is driven to low (no current through D1) the TLE 4261 is still active, because the voltage level at point A is at 5 V. From this moment on the voltage regulator is controlled solely by the port pin P5.4. The running software is now able to delay the "switch off" for the TLE 4261 until all necessary data have been written into the internal RAM. Once this writing sequence is finished, the port pin P5.4 is set to high. Thus, the transistor is switched on and pulls the collector voltage down to 0 V. This disables the regulator via the INH pin.

The main power supply

Before going on with the description of the circuit layout, a short look at the interdependency of the status line and supply line is provided. For this application example a power supply is used which indicates a power breakdown by setting the status line to low. The status line is also low when the output voltage falls under a defined limit. In normal operation the output voltage is 12 V. In this case the status line is inactive (10 V). If the output voltage falls under the limit of 9 V (e.g. switch off or short connection) the status line indicates this by going to low. As the output is buffered by a big capacitor, the changing of the output voltage is controlled by the following formula:

dt = (C * dU)/I
dt = delta time [s]
C = capacity [F]
dU = delta voltage [V]
I = current [A]

However the problem is that the voltage regulator TLE 4261 itself needs a minimum input voltage (pin 1) of 5.5 V to guarantee an output voltage of 5 V. The time between the low at the status line and the point at which the critical limit of 5.5 V at the supply line is reached, is thus of significance. Exactly this time is available for updating the internal RAM and also for going into hardware power down (to be discussed later). The following is an estimation of time available.

dt = (C * dU/I

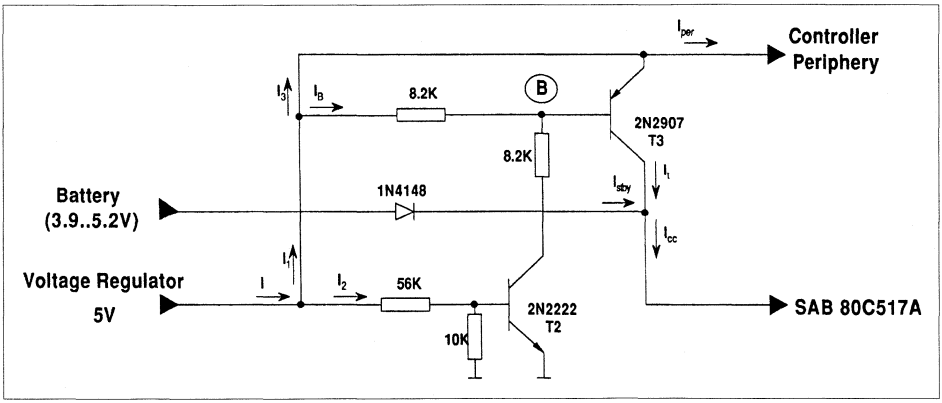
Typical values are: C = 10000 µF, dU = 3.5 V (9 V – 5.5 V), I = 1 A

When these values are used for the formula, the result is a time span of 35 ms. This is sufficient enough to carry out a complete update of the internal RAM (2304-bytes), and a few more lines of code (including the converting time of the Analog Digital Converter and jump into hardware power down).

Additionally, some bus systems (VME-bus, Multibus I and II) provide an ACFAIL-Signal. This signal can also be used as a status line.

The supply switch

The main difference between application example No. 1 and No. 2 lies in the concept of the supply switch. In the previous example this unit was located outside the controller board. In application example No. 1 the supply line used was constantly active. In normal operation the board was served by a generator and in standby by a battery. However, in application example No. 2 the supply line is inactive in standby mode. For this reason the battery and the supply switch are located "on-board".



When and how does the supply switch become active

In normal operation mode the voltage regulator is active and the voltage output pin (pin 7) of the TLE 4261 provides currents I_1 and I_2. The slight current I_2 is needed to switch on the NPN-transistor T2 (I_2 approx. 80 µA) and thus pull the voltage level down to 0.2 V at point B. At the PNP-transistor T3 the current I_3 is split into the current for the controller periphery (I_{per}) and the transistor current (I_t). Due to the low level at the base of T3 an emitter base current causes an emitter collector current (I_t minus emitter base current). This current is the supply current for the SAB 80C517A (I_{CC}) in normal operation mode. The supply current for the SAB 80C517A is lower than 40 mA with a controller clock of 18 MHz. In normal operation the standby current I_{stby} is 0 A.

When the voltage regulator TLE 4261 is switched off two things happen. Firtly the supply switch becomes active and secondly the SAB 80C517A must be forced into Hardware-power-down mode.

If the status line indicates standby mode, the delay control becomes active and the TLE 4261 is turned off via the INH pin. As a result the output voltage of the regulator drops down from 5 V to 0 V (buffered by a 22 µF capacitor). This occurs when the supply switch becomes active. Due to the absence of 5 V at pin 7 of the TLE 4261, the transistor T2 is switched off (I_2 = 0 A) and also results in $I_3 = I_B$ = 0 A. In this case the transistor is turned off (I_t = 0) and the controller's periphery is also turned off. From this moment on the controller's supply current is provided by the battery (e.g. lithium battery). To guarantee a minimum supply current the SAB 80C517A must be in Hardware-power-down.

The branch into Hardware-power-down occurs in the following way. The reset pin of the TLE 4261 (pin 3) is connected with the HWPD# pin of the SAB 80C517A. A logical low at this line carries out the internal power down sequence of the SAB 80C517A (see **figure 1**). In normal operation mode (TLE 4261 active) the reset pin of the TLE 4261 is inactive (pulled up with 10 Kohm) and the level at the HWPD# pin is also high. When the output voltage of the TLE 4261 drops below 4.7 V the reset pin becomes active and forces the SAB 80C517A into Hardware-power-down. The same happens if the regulator is switched off by the INH pin. As soon as the SAB 80C517A detects a low level at the HWPD# pin, it takes approximately 1.8 µs for Hardware-power-down to be reached. During this time the normal supply current (40 mA) is required. After this, the consumption is reduced to below 50 µA and all ports are switched into tri-state. From this moment on the controller is completely disconnected from its environment.

Finally a few words about the standby source.

For the standby source a lithium battery - for example - can be used. The typical cell voltage of this battery is 1.3 V. To realize data saving in the internal RAM of the SAB 80C517A in Hardware-power-down mode the supply voltage should not fall below 2 V. This results in the requirement of three (3.9 V) or four (5.2 V) cells. If a diode with a junction voltage of less than 0.6 V is used, it is also possible to use only two cells (2.6 V).

There are a few things to bear in mind about replacing the lithium batteries when the main power supply is switched off. The SAB 80C517A tries to execute a power on reset, because the V_{CC} pin is now supplied. When two or three cells are used, the actual supply voltage does not reach the value for normal operation mode (V_{CC} = 5 V +/– 10%). The SAB 80C517A is then in an undefined state. To avoid this, the main power supply must be turned on immediately after the replacement of the battery.

Another alternative is to take four lithium cells (5.2 V). If the battery is now replaced, the supply voltage of the SAB 80C517A is within the range of normal operation. Thus the power on reset is successful (restart of the SAB 80C517A in 18 µs). After this restart the internal statemachine executes the power-down mode (HWPD#-pin is still low) and the power consumption is reduced to less than 50 µA.

Figure 10

```
$DEBUG
$SYMBOLS
$ERRORPRINT
$DATE (JAN-25-91)
$NOMOD51
$INCLUDE (REG517.PDF)

;APPLICATION SAB80C517A IN HARDWARE-POWER-DOWN

;
;**************DECLARATION*****************************************
;

                CSEG AT RESET
                LJMP START

START:          CLR     EAL             ; DISABLE ALL INTERRUPTS
;
;**************TIMER 1*********************************************
;
                MOV     TMOD,#10H               ; SET TIMER 1 MODE
                CLR     ET1                     ; CLEAR TIMER 1 INTERRUPT
                CLR     TF1                     ; CLEAR OVERFLOW BIT
                CLR     TR1                     ; STOP TIMER 1
;
;**************A/D CONVERTER***************************************
;
                MOV     ADCON0,#01H     ; CONFIGURATION OF THE A/D CONVERTER
                CLR     IADC                    ; DISABLE A/D INTERRUPT
;
;**************MAIN************************************************
;
                ANL     P5,#0EFH                ; SET DELAY-CONTROL
I0001:          MOV     DAPR,#00H       ; START A/D CONVERTER
I0002:          JB      BSY,I0002       ; CHECK BUSY-FLAG
                MOV     A,ADDAT                 ; READ VALUE
                MOV     B,#04H          ; DEFINE RANGE
                DIV     AB
                JZ      I0003           ; IF LOW-LEVEL JUMP TO I0003
                SJMP    I0001
```

```
I0003:  MOV   R4,#8DH      ; LOAD LOOP-COUNTER
        ANL   P5,#0FAH             ; SET MONITOR-BIT
I0005:  CLR   TF1          ; CLEAR OVERFLOW-FLAGT
        MOV   TL1,#00H             ; START-VALUE FOR TIMER 1
        MOV   TH1,#00H             ; ----------"----------
        SETB  TR1                  ; START TIMER 1
I0004:  JNB   TF1,I0004    ; CHECK OVERFLOW-FLAG
        CLR   TR1
        DJNZ  R4,I0005
        ANL   P5,#0F0H             ; SET MONITOR-SIGN
I0006:  ORL   P5,#10H      ; CLEAR DELAY-CONTROL
        SJMP  I0006
        END
```

SIEMENS

Application Note

E^2PROM Interface with a Siemens 8031 based Microcontroller

This application note provides users with a solution to interface an E^2PROM to an 8031 based microcontroller over the I^2C bus. In this application example, a Siemens microcontroller the SAB 80535 and a Siemens E^2PROM the SDA 2526 or the SDA 2516 are used.

Microcontroller Group 06/88

E²PROM Interface with the SAB 80515/535

Abstract

An on-chip Electrically Erasable Programmable Read-Only Memory (E²PROM) in a microcontroller becomes a very useful peripheral because it allows the system parameters to be stored and reprogrammed without having to remove the microcontroller from the board. An E²PROM can also store internally the system specific information and can quite often replace a battery backed-up CMOS RAM. The write-cycle time of an E²PROM is considerably longer than that of most RAM chips and therefore the device is referred to as a "read-only" memory. Most E²PROMs have a limited number of write/erase endurance cycles and for this reason alone an on-chip E²PROM in a microcontroller is sometimes not desirable. However, Siemens microcontrollers do not have an on-chip E²PROM. Therefore, the user either has to rely on an external E²PROM chip or perform the same function by battery back-up to the microcontroller's internal RAM.

The following application example offers the users a solution of interfacing an E²PROM to a Siemens microcontroller over a two line I²C interface.

Inter-Integrated Circuit Bus

The Inter-Integrated Circuit (I²C) bus is a mechanism for serially communicating with peripheral devices. The bi-directional bus consists of two wires, and it can support multiple masters and operate at various data rates.

The physical part of an I²C interface is a set of two wires, the serial clock (SCL) line and the serial data (SDA) line. The clock line is used to clock data out of a transmitting device into a receiving device. The data line is used to carry the data bits from a transmitting device to a receiving device. It is also used to transfer the acknowledge signal from a receiving device to a transmitting device. When transferring address, data or acknowledge bits the SDA line can change its state only while the clock is low. If the data line changes from high to low while the SCL line is high, a start condition is initiated. A change from low to high while the SCL line is high initiates a stop condition. The basic relationship between the SCL and SDA lines is shown in figure 1.

Hardware

Figure 2 illustrates the hardware interface between a Siemens microcontroller such as the SAB 80535 and a Siemens E²PROM such as the SDA 2526 or the SDA 2516. The bit manipulation capability of the SAB 80515/535 allows any two port pins of the microcontroller to be used for the E²PROM with an I²C bus interface. In this example, port pin P1.0 is used for the SDA line and port pin P1.1 is used for the SCL line of the I²C bus. One could select any two port pins for the interface by making an appropriate change in the software.

Via the I²C bus the memory is controlled by the microcontroller (master) during two operating modes:
a) Read-out cycle.
b) Reprogramming cycle or the write cycle.

In both operating modes the microcontroller has to provide 3 bytes and an additional acknowledge clock on the bus after the start condition. These three bytes contain information like chip select for data input, memory word address and chip select for data output. For more information on the operation of the SDA 2526 or the SDA 2516, please refer to their data-sheets.

Software

The software listing of the subroutines used to read and program (write) the SDA 2526 or the SDA 2516 is attached.

The subroutine Re_EEPROM allows the user to read the E^2PROM. The following parameters need to be transferred to this subroutine to complete the read operation successfully.
a) Register R1 holds the starting address of the E^2PROM.
b) Register R2 holds the number of bytes to be read.
c) Register R0 holds the destination address in the internal RAM of the SAB 80535.

The subroutine Pr_EEPROM allows the user to program the E^2PROM. After programming a byte, the software executes a time delay of about 30 ms (worst case programming duration for the SDA 2526 or the SDA 2516) before writing the next byte. Registers R0, R1 and R2 need to be programmed with the following values before calling this subroutine.
a) Register R1 holds the starting address of the E^2PROM.
b) Register R2 holds the number of bytes to be programmed.
c) Register R0 holds the source address of the data in the internal RAM of the SAB 80535.

References

i) Siemens SAB 80515/535 User's Manual.
ii) Siemens SDA 2526/2516 Data Sheets.
iii) Siemens I^2C Bus Driver Subroutines by R. Mirthes and P. Walter.

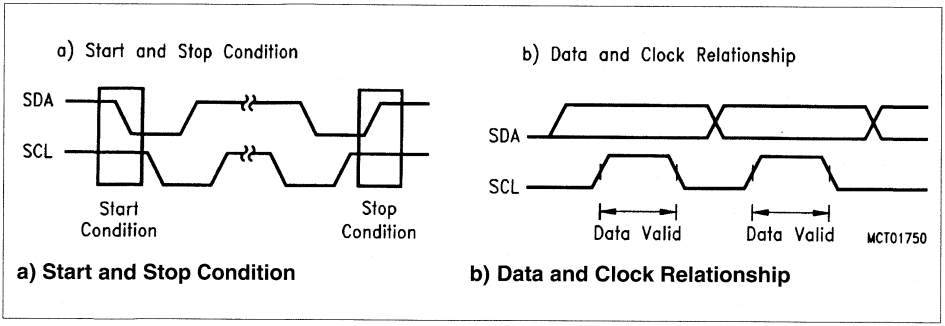


Figure 1. I²C Bus Basic Timing

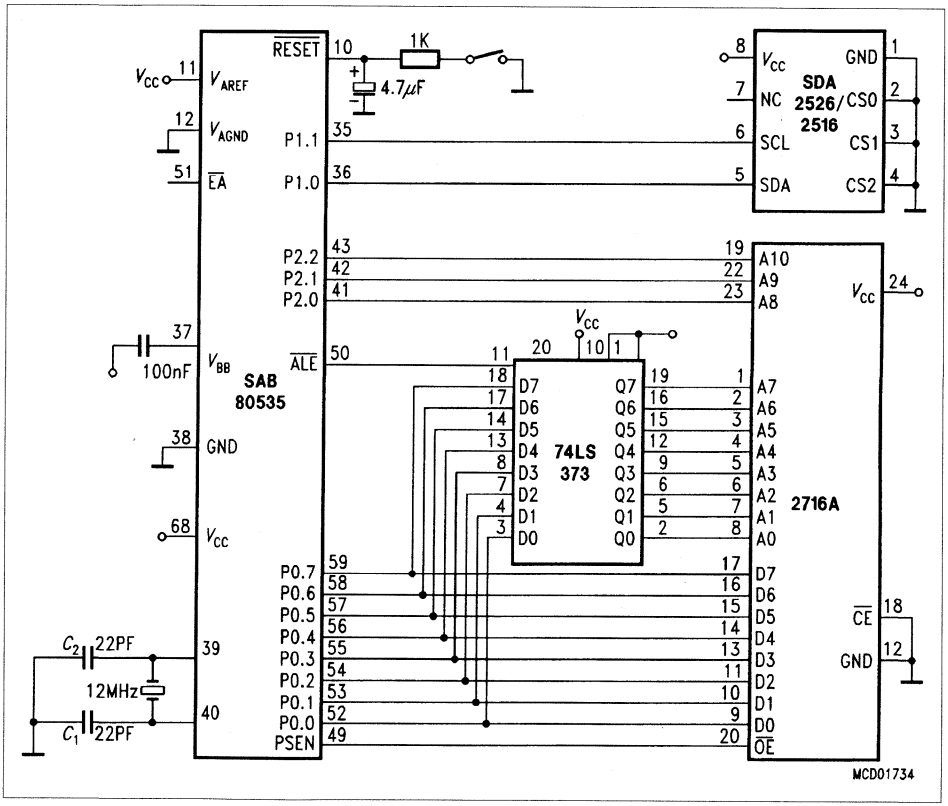


Figure 2. Schematic Diagram

```
                  1   $MOD515
                  2   $PAGELENGTH(80)
                  3   $TITLE          (SAB 80515/80535 IIC-BUS Software for SDA 2526/2516)
                  4
                  5
                  6
0020              7   FLAGS           Data        20H
0021              8   Scratch1        Data        21H
0022              9   Scratch2        Data        22H
0023             10   Scratch3        Data        23H
                 11
0090             12   SDA             Bit         P1.0
0091             13   SCL             Bit         P1.1
0000             14   AckFlag Bit     FLAGS.0
                 15
00A1             16   Adr_EEPROM_L    EQU         10100001B
00A0             17   Adr_EEPROM_S    EQU         10100000B
                 18
                 19   ;*********************************************************************
                 20   ;*                                                                   *
                 21   ;* Program Name : IICSDA                                             *
                 22   ;* Function : This program has the subroutines to read and write     *
                 23   ;*            the Siemens EEPROMs - the SDA 2526 or the SDA 2516.    *
                 24   ;*                                                                   *
                 25   ;*********************************************************************
                 26
0000             27         Org      0
                 28
00               29   Main_Program:
                 30
0000 80FE        31         Sjmp     $
                 32
                 33   ;*********************************************************************
                 34   ;*                                                                   *
                 35   ;* Subroutine_Name : Re_EEPROM                                       *
                 36   ;* Function : This subroutine is called to read the EEPROM. The      *
                 37   ;*            number of bytes to be read are loaded in register R2   *
                 38   ;*            Register R1 holds the starting address of the          *
                 39   ;*            location in the EEPROM. Register R0 holds the          *
                 40   ;*            destination address of RAM in the microcontroller.     *
                 41   ;*                                                                   *
                 42   ;*********************************************************************
                 43
0002             44   Re_EEPROM:
0002 1200D5      45         Call     SaveParam       ; Save input parameters
                 46
0005             47   Read_EEPROM:
0005 1200DC      48         Call     RestoreParam    ; Restore input parameter
0008 74A0        49         Mov      A,#Adr_EEPROM_s
000A 12002A      50         Call     Cs_EEPROM       ; EEPROM chip select
000D 4011        51         Jc       Re_EEPROM_exit  ; Device not available
                 52
```

```
000F 74A1      53          Mov     A,#Adr_EEPROM_L ; C/S for data O/P out of memory
00 120052      54          Call    Start_IIC       ; Initialize with the address
00 40EF        55          Jc      Read_EEPROM     ; If error then repeat
               56
0016           57    Read_loop:
0016 D200      58          Setb    AckFlag         ; Acknowledge flag
               59
0018           60    Lastbyte:
0018 DA09      61          Djnz    R2,Re_EEPROM_Loop
               62
001A C200      63          Clr     AckFlag         ; It is the last byte
001C 1200B0    64          Call    Datain          ; Read databyte in
001F F6        65          Mov     @R0,A           ; Read databyte in internal RAM
0020           66    Re_EEPROM_Exit:
0020 020070    67          Jmp     Stop_IIC        ; Stop_IIC condition
               68
0023           69    Re_EEPROM_Loop:
0023 1200B0    70          Call    Datain          ; Read databyte in
0026 F6        71          Mov     @R0,A           ; Read databyte in internal RAM
0027 08        72          Inc     R0              ; Inc data pointer
0028 80EE      73          Jmp     Lastbyte        ; Read next byte
               74
               75    $EJ
               76    ;*********************************************************************
               77    ;*                                                                   *
               78    ;* Subroutine_Name : Cs_EEPROM                                       *
               79    ;* Function : This subroutine creates a start condition & sends      *
               80    ;*            out the device address and the memory word address     *
               81    ;*            to the SDA 2526/2516. Register R1 contains the add-    *
               82    ;*            ress. If the device is not available the carry flag    *
               83    ;*            is set as an error condition.                          *
               84    ;*                                                                   *
               85    ;*********************************************************************
               86
002A           87    Cs_EEPROM:
002A 120052    88          Call    Start_IIC       ; Start condition & device address
002D 4006      89          Jc      Cs_EEPROM_Exit  ; Device not available
002F E9        90          Mov     A,R1            ; Memory word address
0030 120085    91          Call    Dataout
0033 40F5      92          Jc      Cs_EEPROM       ; If error, repeat
0035           93    Cs_EEPROM_Exit:
0035 22        94          Ret
               95
```

```
                  96   ;*********************************************************************
                  97   ;*                                                                   *
                  98   ;* Subroutine_Name : Pr_EEPROM                                       *
                  99   ;* Function: This subroutine is called to program the EEPROM.        *
                 100   ;*           The # of bytes to be programmed is loaded in R2. R1      *
                 101   ;*           holds the address of the first byte in _EEPROM. R0       *
                 102   ;*           holds the address of the first byte in internal RAM     *
                 103   ;*           of the microcontroller.                                 *
                 104   ;*                                                                   *
                 105   ;*********************************************************************
                 106
0036             107   Pr_EEPROM:
0036 74A0        108         Mov       A,#adr_EEPROM_s
0038 112A        109         Call      Cs_EEPROM        ; EEPROM chip select
003A 4015        110         Jc        Pr_EEPROM_exit   ; Device not available
003C E6          111         Mov       A,@R0            ; Load data byte
003D 120085      112         Call      Dataout
0040 40F4        113         Jc        Pr_EEPROM        ; If error, repeat
0042 120070      114         Call      Stop_IIC         ; Stop_IIC condition
0045 7B64        115         Mov       R3,#100          ; 30 ms wait
0047             116   Wait_Loop:
0047 7C96        117         Mov       R4,#150
0049 DCFE        118         Djnz      R4,$
004B DBFA        119         Djnz      R3,Wait_Loop
004D 08          120         Inc       R0
004E 09          121         Inc       R1
004F DAE5        122         Djnz      R2,Pr_EEPROM     ; Next byte
0051             123   Pr_EEPROM_Exit:
0051 22          124         Ret
                 125
                 126   ;*********************************************************************
                 127   ;*                                                                   *
                 128   ;* Subroutine_Name : Start_IIC                                       *
                 129   ;* Function : Creates a start condition on the I2C bus & then puts*
                 130   ;*            the device address from the accumulator on to the      *
                 131   ;*            bus. After three trials if no acknowledge results      *
                 132   ;*            from the device then the carry flag is set as an       *
                 133   ;*            error condition.                                       *
                 134   ;*                                                                   *
                 135   ;*********************************************************************
                 136
0052             137   Start_IIC:
0052 7C03        138         Mov       R4,#3            ; Maximum 3 adressing attempts
0054             139   Init_IIC:
0054 D290        140         Setb      SDA
0056 1200AA      141         Call      Wait_6
0059 D291        142         Setb      SCL
005B 1200AA      143         Call      Wait_6            ; wait
005E C290        144         Clr       SDA               ; Start condition
0060 1200AA      145         Call      Wait_6            ; wait
0063 C291        146         Clr       SCL
```

```
0065 1200AA  147          Call     Wait_6
0068 120085  148          Call     Dataout          ; Send device address
006B 5002    149          Jnc      Init_IIC_Exit    ; Acknowledge received
006D DCE5    150          Djnz     R4,Init_IIC      ; Next addressing attempt
006F         151    Init_IIC_Exit:
006F 22      152          Ret
             153    $EJ
             154    ;*********************************************************************
             155    ;*                                                                   *
             156    ;* Subroutine_Name : Stop_IIC                                        *
             157    ;* Function : This subroutine creates a stop condition on the IIC *
             158    ;*            bus. Then the status of the SDA line is checked - if*
             159    ;*            low then clock pulses are sent out until SDA line   *
             160    ;*            goes high.                                          *
             161    ;*                                                                   *
             162    ;*********************************************************************
             163
0070         164    Stop_IIC:
0070 C291    165          Clr      SCL
0072 1200AA  166          Call     Wait_6
0075 C290    167          Clr      SDA
0077 1200AA  168          Call     Wait_6
007A D291    169          Setb     SCL
007C 1200AA  170          Call     Wait_6
007F D290    171          Setb     SDA
             172
0081         173    IsSDALow:
0081 3090EC  174          Jnb      SDA,Stop_IIC     ; SDA is not high
0084 22      175          Ret
             176
             177
             178    ;*********************************************************************
             179    ;*                                                                   *
             180    ;* Subroutine_Name : Dataout                                         *
             181    ;* Function : This subroutine transmits a databyte on the IIC bus *
             182    ;*            from the accumulator. The carry flag is set if an   *
             183    ;*            error results.                                      *
             184    ;*                                                                   *
             185    ;*********************************************************************
             186
0085         187    Dataout:
0085 7F08    188          Mov      R7,#8            ; 8 bits in a byte
             189
0087         190    Dataout_Loop:
0087 33      191          Rlc      A
0088 9290    192          Mov      SDA,C            ; Send data bit out
008A 00      193          Nop
008B D291    194          Setb     SCL              ; Set the clock bit
008D 1200AA  195          Call     Wait_6
0090 C291    196          Clr      SCL
0092 1200AA  197          Call     Wait_6
0095 DFF0    198          Djnz     R7,Dataout_Loop
```

```
0097 33        199          Rlc       A
0098 D290      200          Setb      SDA
009A 00        201          Nop
009B D291      202          Setb      SCL              ; Clock pulse for acknowledge
009D 1200AA    203          Call      Wait_6
00A0 A290      204          Mov       C,SDA            ; Get acknowledge bit
00A2 C291      205          Clr       SCL
00A4 1200AB    206          Call      Wait_36
00 40C7        207          Jc        Stop_IIC
00 22          208          Ret
               209
               210    ;*************************************************************************
               211    ;*                                                                       *
               212    ;* Subroutine_Name : Wait_6, Wait_36                                     *
               213    ;* Function : These subroutines cause delays.                            *
               214    ;*                                                                       *
               215    ;*************************************************************************
               216
00AA           217    Wait_6:
00AA 22        218          Ret
               219
00AB           220    Wait_36:
00AB 7B06      221          Mov       R3,#6
00AD DBFE      222          Djnz      R3,$
00AF 22        223          Ret
               224
               225    $EJ
               226    ;*************************************************************************
               227    ;*                                                                       *
               228    ;* Subroutine_Name : Datain                                              *
               229    ;* Function : This subroutine reads a databyte from the IIC bus          *
               230    ;*            into the accumulator. If the AckFlag was set as            *
               231    ;*            this subroutine was called then an acknowledge is          *
               232    ;*            given out during the 9TH clock pulse.                      *
               233    ;*                                                                       *
               234    ;*************************************************************************
               235
00B0           236    Datain:
00B0 D290      237          Setb      SDA
00B2 00        238          Nop
00B3 7F08      239          Mov       R7,#8            ; 8 bits
               240
00B5           241    Datain_Loop:
00B5 D291      242          Setb      SCL              ; Clock pulse
00B7 11AA      243          Call      Wait_6
00B9 A290      244          Mov       C,SDA
00BB 33        245          Rlc       A
00BC C291      246          Clr       SCL
00BE 11AA      247          Call      Wait_6
00C0 DFF3      248          Djnz      R7,Datain_Loop   ; Next bit
               249
```

```
00C2 D290    250          Setb     SDA
00C4 11AA    251          Call     Wait_6
00C6 300002  252          Jnb      AckFlag ,No_Ack
00C9 C290    253          Clr      SDA
             254
             255     No_Ack:
00CB 11AA    256          Call     Wait_6
00CD D291    257          Setb     SCL
00CF 11AA    258          Call     Wait_6
00D1 C291    259          Clr      SCL
00D3 80D6    260          Jmp      Wait_36
             261
             262     ;*********************************************************************
             263     ;*                                                                   *
             264     ;* Subroutine_Name : SaveParam                                       *
             265     ;* Function : This subroutine saves registers R0, R1 & R2.           *
             266     ;*                                                                   *
             267     ;*********************************************************************
             268
00D5         269     SaveParam:
00D5 8821    270          Mov      Scratch1,R0
00D7 8922    271          Mov      Scratch2,R1
00D9 8A23    272          Mov      Scratch3,R2
00DB 22      273          Ret
             274
             275     ;*********************************************************************
             276     ;*                                                                   *
             277     ;* Subroutine_Name : RestoreParam                                    *
             278     ;* Function : This subroutine restores the registers.                *
             279     ;*                                                                   *
             280     ;*********************************************************************
             281
00DC         282     RestoreParam:
00DC A821    283          Mov      R0,Scratch1
00DE A922    284          Mov      R1,Scratch2
00E0 AA23    285          Mov      R2,Scratch3
00E2 22      286          Ret
             287
             288          End
ASSEMBLY COMPLETE, 0 ERRORS FOUND
```

Implementation of the ISDN Oriented Modular (IOM) Interface using the SAB 80515/80535 Microcontroller

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This application note describes how any two port pins of the SAB 80515/535 microcontroller can be programmed to perform the data transmit and receive line functions of the ISDN Oriented Modular (IOM) interface.

Digitization of telephone networks not only increase transmission rates but allow more than one signal to be sent over a telephone line simultaneously. This capability to offer voice and a multiplicity of data services over one network with standard interfaces and call set-up procedures is the real driving force behind today's telecom/datacom revolution.

This one network is called ISDN - the Integrated Services Digital Network.

Integrated	Telecommunication and datacommunication services together on one system.
Services	Voice, data, text, picture, video, telex, facsimile, telemetry, alarms, and more.
Digital	Digital transmission from end to end, with voice digitization handled at the terminal.
Network	One worldwide network, based on existing public telephone lines, providing standard interfaces and call procedures familiar to everyone.

ISDN-Standards For Interconnectability

The international Telegraph and Telephone Consultative Committee (CCITT) has published a series of recommendations that have become the industry standard. These recommendations include ISDN definitions for two different groups of transmission speeds:

Basic Access Rate - 144 Kbits/s user information.
Basic access is configured as two 64 Kbits/s B-channels for voice or data transmission and one 16 Kbits/s D-channel for signalling or packet switched data. This is abbreviated as 2xB + D. It is used to connect voice/data terminals to either a private branch exchange (PBX) or directly to the public central office exchange (CO).

Primary Access Rate - 1.544 Mbits/s user information in USA & Japan.
Primary rates are used to transmit large amounts of data. The increased transmission rate helps to reduce the time of transmission and hence the cost of transmission. 64 Kbits/s channels are configured as 23xB + D in USA/Japan.

Siemens provides a number of dedicated solutions in the form of devices, system integration and software for ISDN. To make the interconnectivity of such ISDN devices possible, Siemens developed the ISDN Oriented Modular (IOM) architecture. The Siemens IOM (rev2) architecture is fast becoming the de-facto standard for telecom designs. Many IC companies (Siemens, AMD, National and AT&T) now support this standard. Although a rich array of devices currently exist to support the bus, the Telecom market is expanding at such a rate that not all applications are covered. It is now Siemens' intent to have IOM interface available on all ISDN devices. Complete ISDN systems from terminals, terminal adapters, network terminators and transmission repeaters to line cards for digital exchange systems can be optimally designed using the IOM family of ICs.

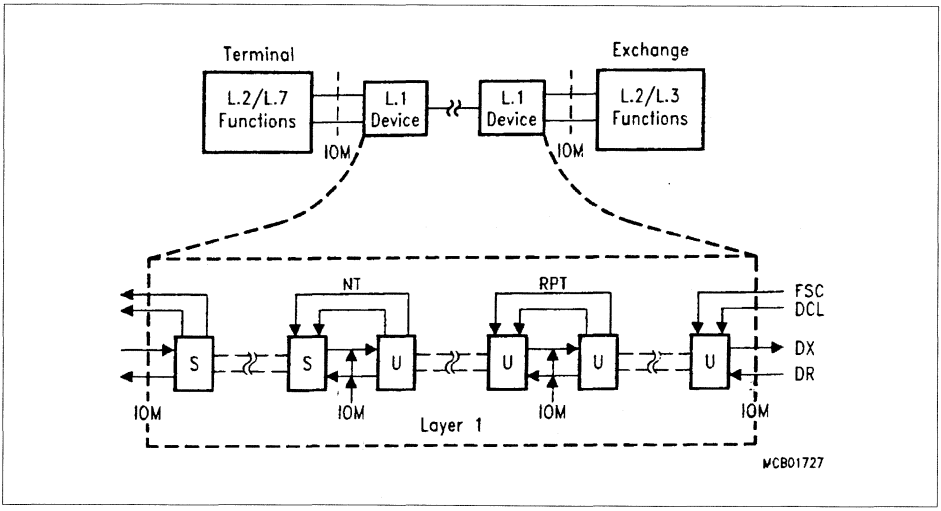


Figure 1. Applications of the IOM-Interface in the Basic Access

ISDN Oriented Modular (IOM) Architecture

The IOM interface is a standard 4-wire local interface for the interconnection of ISDN-devices within the ISDN basic access. It consists of a receive and a transmit data line, an 8-KHz frame signal (FSC) and a 512 KHz data clock signal (DCL). The interface is tailor-made to fit the needs of the ISDN basic access. Typical applications shown in figure 1 are:

In a repeater; two identical transmission devices are set back-to-back to achieve an increase in range.
In an NT (Network Termination); two different transmission devices are combined to convert between the S and U interface.
In the terminal (TE) and the exchange; the IOM interface interlinks the layer 1 and layer 2 device. In addition to the point to point configuration, the IOM-interface can support a point-multipoint configuration.

In all applications the ISDN data rate of 144 Kbit (2xB + 1xD) has to be transferred across the IOM interface transparently. In addition, there is a need for the exchange of control information for activating/deactivating layer 1 and for switching test loops. A few applications require further capacity to transfer maintenance information via this interface. All this information is transferred in a time-division multiplexed mode based on an 8-KHz frame structure (figure 2) and assigned to the following four octets per frame and direction:

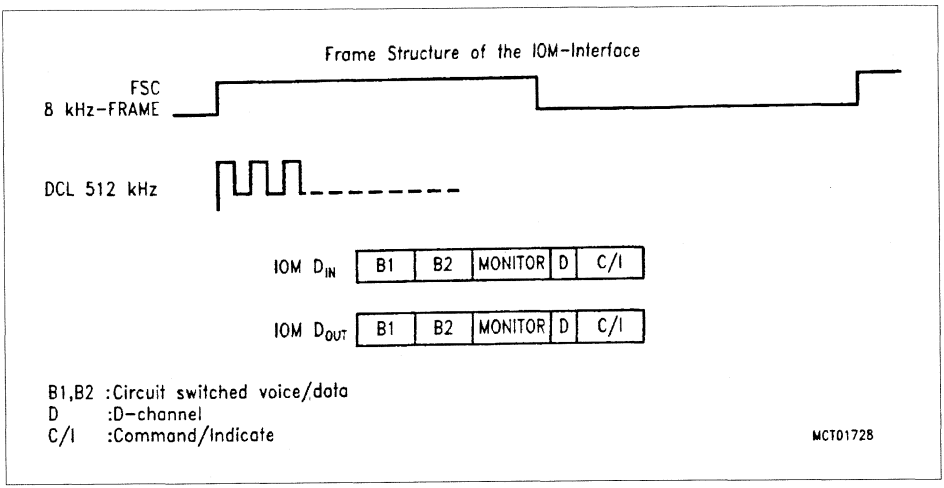


Figure 2

The 64 Kbits/sec channels B1 and B2 occupy the first two octets.
The third octet (monitor channel) is used for transferring the maintenance information.
The two D-channel bits, the four Command/Indicate-bits (which control the activation/deactivation procedure), the T-bit and the E-bit are transferred in the fourth octet. The E-bit supports the handling of the monitor channel and the T-bit is reserved for a transparent 1K-bit channel.

These four octets per frame constitute a bit rate of 256 Kbps. The transmission rate depends on one of the following modes:

Normal mode: data rate: 256 Kbps
bit rate: 256 Kbps
clock frequency: 512 KHz

Mux mode: data rate: 256 Kbps
bit rate: 2.048 Mbps
clock frequency: 4.096 MHz

In the multiplex mode the outputs of up to eight layer 1 devices may be connected together to form an eight-time-slot IOM interface bus with a 2 MHz data rate. The physical timing of the IOM-interface in different modes is shown in figure 3.

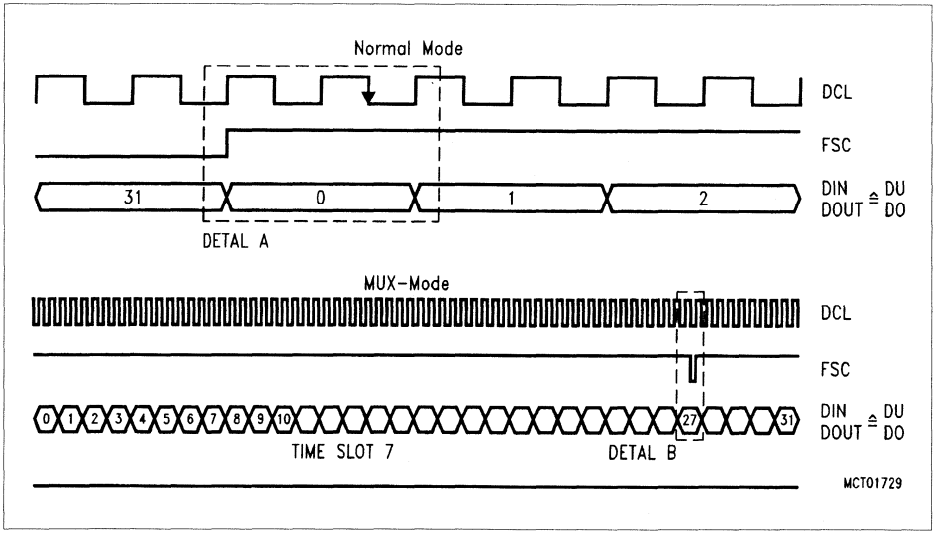


Figure 3. IOM Interface Timing

SAB 80515/535 Role

The primary role of the SAB 80515/535 microcontroller in generating the IOM interface in normal mode is to accept the frame synchronization (FSC) signal as an input and based on this signal identify the four octets on the receive and transmit data lines. Any two port pins of the SAB 80515/535 can be used as the transmit and receive data lines. The PTRA unit of the SAB 80515/535 plays a major role not only in defining the octets but also in generating and receiving the data bit stream over the transmit and receive lines in synchronization with the frame and data clock signals. In this respect the SAB 80515/535 falls into a unique family of microcontrollers which can perform this function.

PTRA Unit of the SAB 80515/535

The Programmable Timer/Counter Register Array (PTRA) of the SAB 80535/515 has a time-base which is a programmable 16-bit timer/counter also known as the Timer 2. Timer 2 is the only one that can serve the PTRA.

The PTRA consists of the following registers:

T2CON	Timer 2 control register
TL2	Timer 2 register, low-byte
TH2	Timer 2 register, high-byte
CRCL	Compare/reload/capture register, low-byte
CRCH	Compare/reload/capture register, high-byte
CCL1	Compare/capture register 1, low-byte
CCH1	Compare/capture register 1, high-byte
CCL2	Compare/capture register 2, low-byte
CCH2	Compare/capture register 2, high-byte
CCL3	Compare/capture register 3, low-byte
CCH3	Compare/capture register 3, high-byte
CCEN	Compare/capture enable register

For brevity, the double-byte Compare/Reload/Capture register is called CRC register, and the three double-byte Compare/Capture registers are called CC registers 1 to 3. The PTRA shares Port 1 pins for hardware interfacing as shown in table 1.

Port Pin	Name	Function
P1.0	INT3 / CC0	Compare output/Capture input for the CRC register
P1.1	INT4 / CC1	Compare output/Capture input for CC register 1
P1.2	INT5 / CC2	Compare output/Capture input for CC register 2
P1.3	INT6 / CC3	Compare output/Capture input for CC register 3
P1.5	T2EX	External Reload trigger input
P1.7	T2	External Count or Gate input to timer 2

Table 1. Hardware Interfacing for the PTRA Unit.

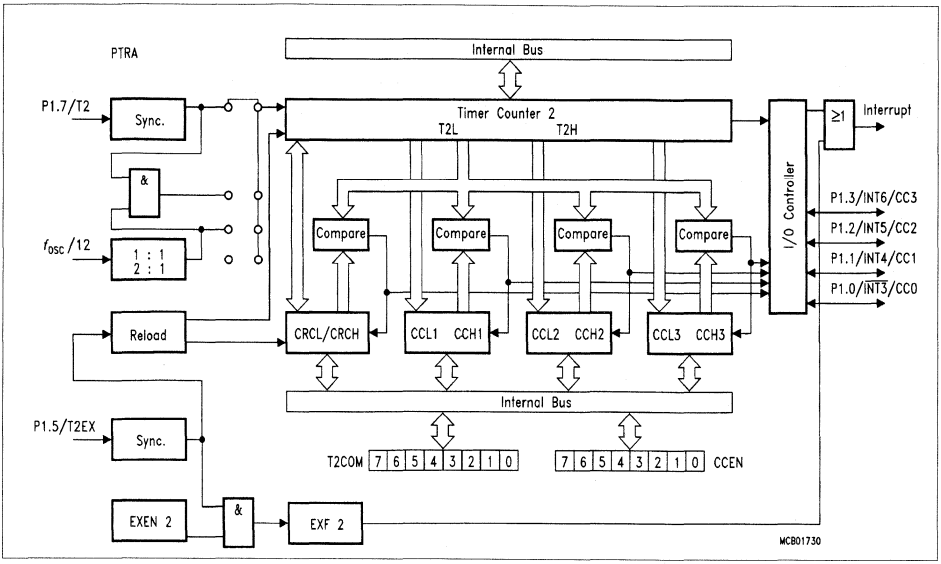


Figure 4. Block Diagram of the PTRA Unit.

In addition to supporting the operational modes of a timer or a counter, the PTRA provides the following features for the Timer 2.

- 16 bit reload
- 16 bit compare
- 16 bit capture

Figure 4 shows a block diagram of the PTRA unit.

The Timer 2 of PTRA can operate either as timer, event counter, or gated timer. In timer mode, the count rate is derived from the oscillator frequency. A 2:1 pre-scaler makes it possible to select a count rate of 1/12 or 1/24 of the oscillator frequency. In either case, no matter whether Timer 2 is configured as timer, event counter, or gated timer; when the count rolls over from all 1's to all 0's it sets the Timer 2 overflow flag which can generate an interrupt. In counter mode, the Timer 2 register is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7).

The reload mode of the PTRA unit allows contents of Timer 2 to be reloaded from the CRC register at the time when Timer 2 rolls over from all 1's to all 0's. The 16-bit reload from the CRC register to Timer 2 registers can also be caused by a negative transition at port pin P1.5.

In the compare mode, the 16-bit values stored in the dedicated compare registers of the PTRA are compared with the contents of the Timer 2 registers TL2 and TH2. If the count value in the Timer 2 register matches the stored value an appropriate output signal is generated at the corresponding port 1 pin, and an interrupt can also be enabled.

In the PTRA compare mode-0, the output signals at port pins P1.1 through P1.3 change from low to high upon a match of the corresponding CC1 through CC3 register contents with contents of the Timer 2 registers. The outputs then go back to a low level on Timer 2 overflow, and Timer 2 restarts by reloading the CRC register contents. In the second mode of operation the output port pins P1.0 through P1.3 can be caused to toggle at compare events, thereby resulting in the generation of square waves at these outputs. In this mode the Timer 2 overflow has no affect on the output port pins. Each of the three compare/capture and the CRC registers of the PTRA unit can be used to latch the current 16-bit value of the timer 2 in one of them. This latching could either be caused by an external event or upon writing to the low-order byte of the dedicated 16-bit capture register. Either a rising or a falling edge can be selected to cause the capture from Timer 2 into the CRC register, whereas for the CC registers 1 to 3 a positive transition causes the capture.

IOM Interface using the SAB 80515/535

The high speed of the SAB 80515/535 microcontroller allows its machine cycle (1/12 of oscillator frequency) to be twice as fast as the DCL which means the microcontroller can easily handle two DCLs per data bit. To achieve this the crystal oscillator frequency is selected at 24 times the data clock i.e., 24 × 512 KHz = 12.288 MHz. As a result, the Timer 2 which is programmed to operate in mode 1 also counts at twice the rate of the data clock. Timer 2 is programmed to increment at the rate of 1024 KHz as opposed to counting at the data clock rate of 512 KHz. Though the latter could be accomplished by connecting the data clock to port pin P1.7 of the microcontroller and letting the Timer 2 count in the external count mode. But this is not desirable as the count rate of 1024 KHz gives a higher resolution for the compare feature. However, the synchronization is achieved by programming the Timer 2 to count at a value of 0FF80H every time the falling edge of the FSC (Frame Synchronization) signal is detected at port pin P1.5. The falling edge of the FSC signal coincides with the occurrence of the first data bit in octet 3 (monitor channel).

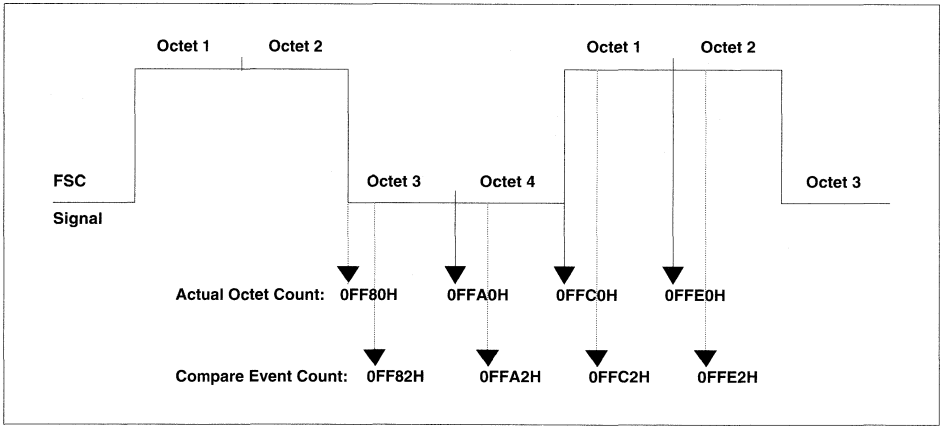


Figure 5. Octet Placement in FSC Signal

With 0FF80H being the start value of Timer 2 which also marks the beginning of third octet, the other octets occur 32 counts apart. This derives from the fact that there are two DCLs per data bit (4 machine cycles or 4 counts per data bit) and there are 8 data bits per octet. Based on this analogy, the octets 3, 4, 1 and 2 occur at the Timer 2 count values of 0FF80H, 0FFA0H, 0FFC0H and 0FFE0H respectively as shown in figure 5. In other words, if the compare interrupt was invoked at these count values, the user will be in the desired octet to transmit or receive a data bit stream. However, the delay involved in processing the interrupt will also delay the occurrence of a data bit at the desired DCL. To understand the compare interrupt handling in the SAB 80515/535, one will first have to understand the basic machine cycle timings of the SAB 80515/535.

A machine cycle consists of 6 states (12 oscillator periods). Each state is divided into two phases - phase 1 and phase 2. Thus a machine cycle consists of 12 phases or 12 oscillator periods, numbered S1P1 (state 1, phase 1) through S6P2 (state 6, phase 2). Each phase lasts for one oscillator period and each state lasts for two oscillator periods. Timer 2 is incremented in S1P1 of every machine cycle. An internal compare signal is generated in S2P2, if Timer 2 increments to the compare count in one of the compare registers CC1 through CC3. The compare signal is active as long as the Timer 2 contents are equal to one of the compare registers. For the compare registers CC1 to CC3 an interrupt is always requested and a flag is set when the compare signal goes active. The interrupt flags are sampled in S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition in S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine. As shown in figure 6 a standard interrupt handling procedure can take about 4 machine cycles. For exceptions please refer to the SAB 80515/535 user's manual.

Based on above facts, in the present application, two DCLs (4 machine cycles) have already elapsed before the program enters into the compare subroutine. To avoid this delay, the compare interrupt subroutine is invoked 30 machine cycles or 15 DCLs before the desired octet. Therefore the compare event for different octets occur at the following count values:

Octet 1, count value = 0FFA2H
Octet 2, count value = 0FFC2H
Octet 3, count value = 0FFE2H
Octet 4, count value = 0FF82H

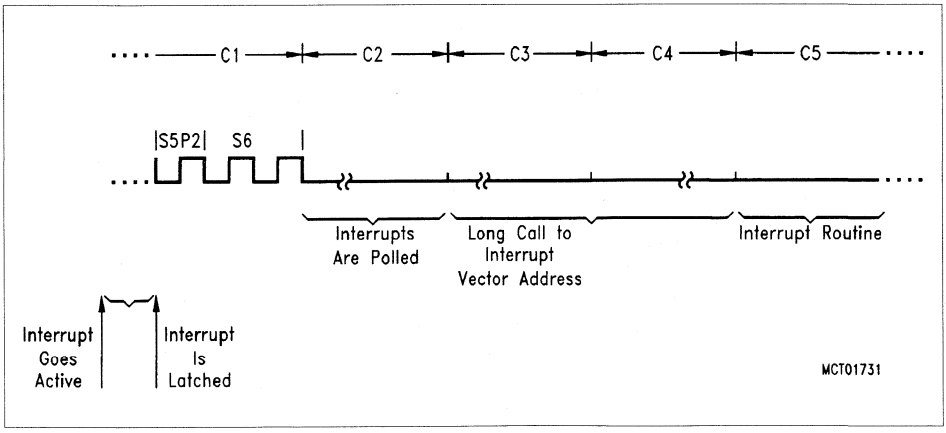


Figure 6. Interrupt Response Timing Diagram.

In either transmit or receive mode, when compare interrupt occurs at one of the above count values, the microcontroller performs no-operation until 30 machine cycles elapse. At that instant, the microcontroller sends out or receives the data bit stream as that is the beginning of the desired octet.

System Inplementation

The program listing (refer to Appendix A) has two subroutines - one for transmit and the other for receive mode. In either case the data variable "count" holds the lower byte of the desired octet to perform the compare match. In transmit mode the data is taken from external memory and in the receive mode the data is stored in the external memory starting at address 0000H. The total time spent in the compare interrupt subroutine to transmit or receive a byte varies from 75 to 82 machine cycles. This variation is caused due to the time spent in deciding whether or not the byte transmitted or received is the last byte. The next byte is not transmitted or received until the next octet in subsequent frame i.e., 128 machine cycles later. Therefore the CPU is free for 128 machine cycles minus the time spent in machine cycles in the compare interrupt subroutine. However more time could be made available for the CPU by cutting down the number of NOPs in the compare interrupt subroutine and by increasing the compare count to compensate for the number of NOPs removed. In that case the compare event could occur as close as 4 machine cycles before the desired octet count.

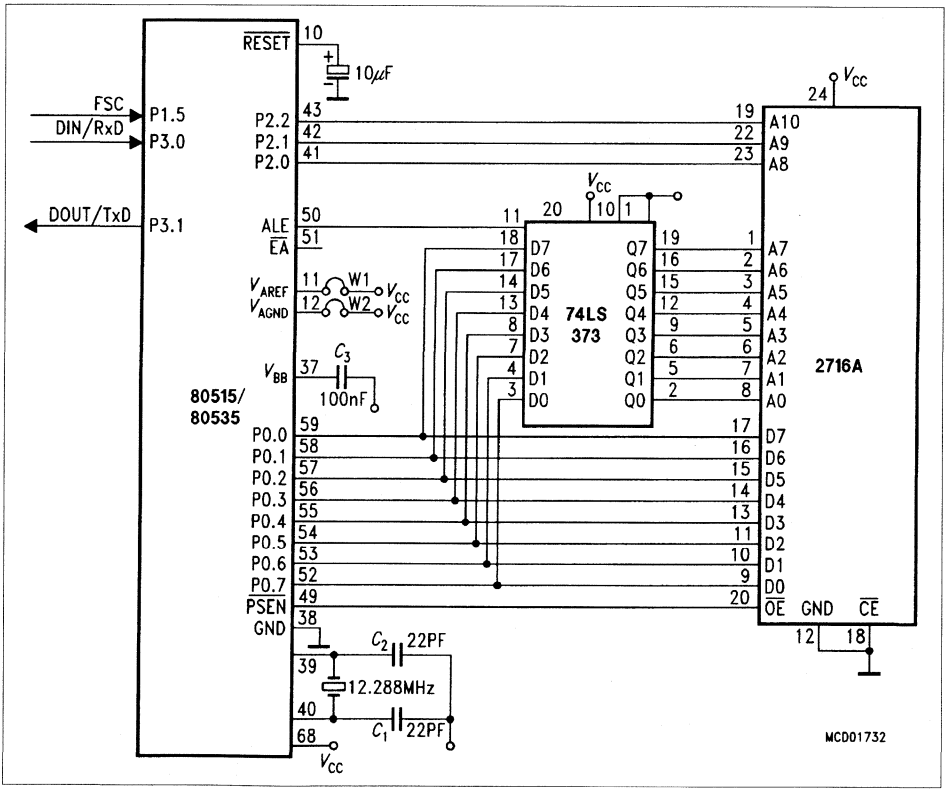


Figure 7. SAB 80535 Schematic Diagram

Any two port pins of the SAB 80515/535 can be used as the data transmit and data receive lines. In this application port pin P3.0 is used as the receive data line and the port pin P3.1 is used as the transmit data line. Figure 7 shows the basic SAB 80535 circuit required to run the subroutines. The pins used for the IOM interface are also shown. The other on-chip peripherals namely the serial port, Timer 0 and Timer 1, the watchdog timer, the A/D converter and 30 I/O lines are still available to perform any other system functions.

Figure 8 shows an ISDN application where the SAB 80515/535 is being used as a terminal interfaced to an ISDN network simulator over the S-interface.

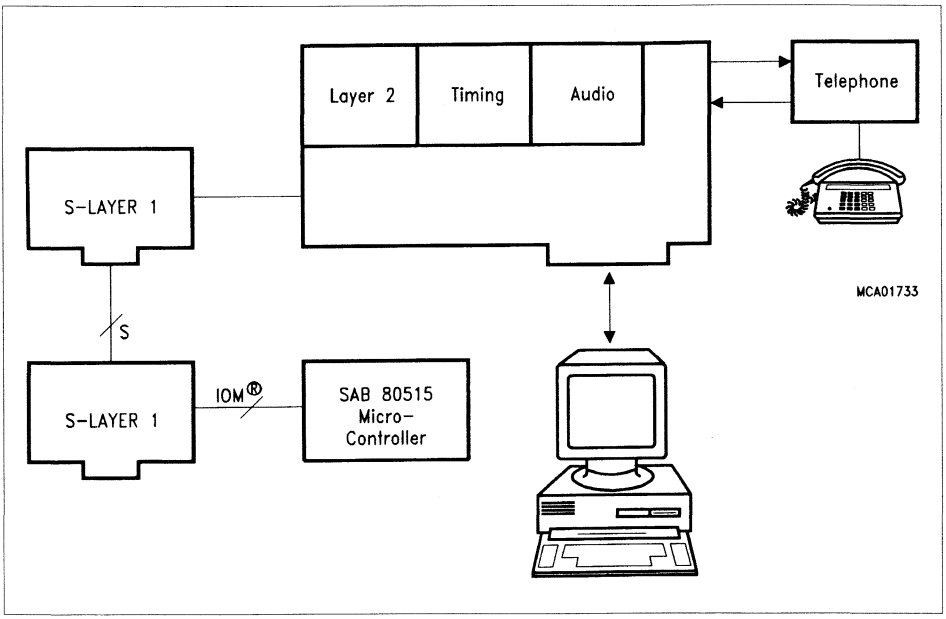


Figure 8. NT-Simulator Application using the SAB 80515/535 as a Terminal

References

1) Siemens, 8-bit Single-chip Microcontroller Handbook, 1989/90.
2) Siemens, Telecommunications Data Book, 1987.
3) Total ISDN Commitment, a Siemens Brochure.
4) Steve Hardwick, Siemens Telecom Applications.

```
                1   $Mod515
                2   $Pagelength(70)
                3   $Debug
                4   $Title (IOM Interface              Appendix A)
                5
                6
                7
                8   ;*********************************************************************
                9   ;* IOM Interface Program:                                            *
               10   ;* In the following program the variable "Count" holds the octet     *
               11   ;* count in which the data byte is to be transmitted. The valid      *
               12   ;* octet counts are: for octet 1, count = 0A2H; octet 2, count =     *
               13   ;* 0C2H; octet 3, count = 0E2H; octet 4, count = 82H. These bytes    *
               14   ;* are stored in the external data memory. The bytes appear in       *
               15   ;* the desired octet in every subsequent frame until the last        *
               16   ;* byte is transmitted. The external crystal oscillator frequency    *
               17   ;* is 12.288 MHz (24 x 512 KHz).                                     *
               18   ;*********************************************************************
               19
               20
               21
00A2           22   Count    EQU     0A2H              ;Octet 1=A2,2=C2,3=E2,4=82.
               23
               24   Cseg     at      0H
               25
0000 020100    26            LJMP    Main_Begin
               27
               28   ;*********************************************************************
               29   ;* Write_IOM_Subroutine:                                             *
               30   ;* The following subroutine happens 30 machine cycles (15 DCLs)      *
               31   ;* before the occurrence of the desired octet. The data byte is      *
               32   ;* output on port bit P3.1 coinciding with the occurrence of the     *
               33   ;* desired octet. The data byte is taken from external memory and    *
               34   ;* the data pointer to external memory is incremented after a byte   *
               35   ;* is transmitted over the IOM interface. The subroutine is exited   *
               36   ;* before the arrival of the falling edge of the FSC at port pin     *
               37   ;* p1.5.                                                             *
               38   ;*********************************************************************
               39
               40
005B           41            Org     5BH               ;Compare 1 interrupt routine.
               42
005B           43   Write_IOM_Subroutine:              ;4 m/c for servicing the routine.
               44
005B C2BB      45            CLR     IEM1.3            ;7th m/c into the frame.
               46
```

```
005D 00      47          NOP                    ;8th m/c into the frame.
005E 00      48          NOP                    ;9th m/c into the frame.
005F 00      49          NOP                    ;10th m/c into the frame.
0060 00      50          NOP                    ;11th m/c into the frame.
0061 00      51          NOP                    ;12th m/c into the frame.
0062 00      52          NOP                    ;13th m/c into the frame.
0063 00      53          NOP                    ;14th m/c into the frame.
0064 00      54          NOP                    ;15th m/c into the frame.
0065 00      55          NOP                    ;16th m/c into the frame.
0066 00      56          NOP                    ;17th m/c into the frame.
0067 00      57          NOP                    ;18th m/c into the frame.
0068 00      58          NOP                    ;19th m/c into the frame.
0069 00      59          NOP                    ;20th m/c into the frame.
006A 00      60          NOP                    ;21st m/c into the frame.
006B 00      61          NOP                    ;22nd m/c into the frame.
006C 00      62          NOP                    ;23rd m/c into the frame.
006D 00      63          NOP                    ;24th m/c into the frame.
006E 00      64          NOP                    ;25th m/c into the frame.
006F 00      65          NOP                    ;26th m/c into the frame.
0070 00      66          NOP                    ;27th m/c into the frame.
0071 00      67          NOP                    ;28th m/c into the frame.
             68
0072 13      69          RRC     A              ;29th m/c into the frame.
0073 00      70          NOP                    ;30th m/c into the frame.
0074 92B1    71          MOV     P3.1,C         ;Two more cycles.
             72
0076 13      73          RRC     A              ;New octet, first bit arrives.
0077 00      74          NOP                    ;34th cycle.
0078 92B1    75          MOV     P3.1,C         ;Second bit sent.
             76
007A 13      77          RRC     A              ;Third bit to carry flag.
007B 00      78          NOP                    ;38th cycle.
007C 92B1    79          MOV     P3.1,C         ;Third bit sent.
             80
007E 13      81          RRC     A              ;Fourth bit to carry flag.
007F 00      82          NOP                    ;42nd cycle.
0080 92B1    83          MOV     P3.1,C         ;Fourth bit sent.
             84
0082 13      85          RRC     A              ;Fifth bit to carry flag.
0083 00      86          NOP                    ;46th cycle.
0084 92B1    87          MOV     P3.1,C         ;Fifth bit sent.
             88
0086 13      89          RRC     A              ;Sixth bit to carry flag.
0087 00      90          NOP                    ;50th cycle.
0088 92B1    91          MOV     P3.1,C         ;Sixth bit sent.
             92
008A 13      93          RRC     A              ;Seventh bit to carry flag.
008B 00      94          NOP                    ;54th cycle.
008C 92B1    95          MOV     P3.1,C         ;Seventh bit sent.
             96
```

```
008E 13        97          RRC     A                ;Eigth bit to carry flag.
008F 00        98          NOP                      ;58th cycle.
0090 92B1      99          MOV     P3.1,C           ;Eigth bit sent.
               100
0092 00        101         NOP                      ;122th DCL (61st cycle).
0093 00        102         NOP                      ;62nd cycle.
0094 00        103         NOP                      ;63rd cycle.
0095 D2B1      104         SETB    P3.1             ;32nd DCL (64th cycle).
               105
0097 A3        106         INC     DPTR             ;Increment the data pointer.
0098 E0        107         MOVX    A,@DPTR          ;Load the acc. with next byte.
0099 A883      108         MOV     R0,DPH           ;To compare if end of array
009B B8FF08    109         CJNE    R0,#0FFH,CONTI   ;Compare the high byte first.
009E A882      110         MOV     R0,DPL           ;Load the lower byte
                                                     for comparison.
00A0 B8FF03    111         CJNE    R0,#0FFH,CONTI   ;Compare the lower byte.
               112
00A3 900000    113         MOV     DPTR,#00H        ;Initialize the data pointer.
               114
00A6           115   CONTI:
00A6 C2C3      116         CLR     IRCON.3
???? D2BB      117         SETB    IEM1.3
00AA 32        118         RETI
               119
               120
               121
               122   ;*********************************************************************
               123   ;* Write_IOM_Set-up:                                                 *
               124   ;* In this program the registers are set up to allow compare to      *
               125   ;* happen at the "count" value. The PTRA unit of the SAB 80535 is    *
               126   ;* programmed in the compare mode 1. The "count" value is assigned   *
               127   ;* to the compare register 1 and the corresponding interrupt is      *
               128   ;* enabled. The Timer 2 of the PTRA unit is programmed to restart    *
               129   ;* at a value of FF80H on the arrival of the falling edge of the     *
               130   ;* FSC signal.                                                       *
               131   ;*********************************************************************
               132
               133
               134
0100           135         ORG     100H
```

```
0100            136   Main_Begin:
0100 900000     137           MOV     DPTR,#00H         ;DPTR = (start of data array).
0103 75C100     138           MOV     CCEH,#00H         ;Disable compare mode.
0106 75B0FF     139           MOV     P3,#0FFH          ;SDO, SDI lines are high.
                140
0109 75C3FF     141           MOV     CCH1,#0FFH        ;Compare register has a value
010C 75C2A2     142           MOV     CCL1,#Count       ;corresponding to the
                                                         octet desired.
010F 75CBFF     143           MOV     CRCH,#0FFH
0112 75CA80     144           MOV     CRCL,#080H        ;Reload = 0FFFFH-128 (32x4).
0115 75CDFF     145           MOV     TH2,#0FFH
0118 75CC81     146           MOV     TL2,#81H          ;To avoid compare at FF80H
0118 D2CA       147           SETB    T2CM              ;T2 in compare mode 1
011D 75C108     148           MOV     CCEN,#08H         ;Compare mode enabled
0120 D2AF       149           SETB    EAL               ;Master interrupt Bit enabled.
                150
0122 758910     151           MOV     TMOD,#10H         ;Timer1 to cause more than
0125 758DFF     152           MOV     TH1,#0FFH         ;quarter of a frame delay
0128 758BD0     153           MOV     TL1,#256-48       ;to avoid match before reload.
                154
012B            155   Start:
012B 2096FD     156           JB      P1.6,$            ;Prepare for start pulse arrival.
012E 3096FD     157           JNB     P1.6,$            ;Wait for the start pulse, 1 m/c.
0131 D28E       158           SETB    TR1               ;So far 2 m/c into the frame.
0133 308FFD     159           JNB     TF1,$             ;Wait for another 49 m/c.
                160
0136 75C81D     161           MOV     T2COM;#1DH        ;T2 auto reload from P1.5.
0139 D2BB       162           SETB    IEM1.3            ;Compare interrupt 1 enable.
                163
013B 213B       164           AJMP    $                 ;Wait for a match.
                165
                166           end
ASSEMBLY COMPLETE, 0 ERRORS FOUND
```

```
                1   $Mod515
                2   $Pagelength(73)
                3   $Debug
                4   $Title (IOM Interface              Appendix A)
                5
                6
                7
                8   ;*********************************************************************
                9   ;* IOM Interface Program:                                            *
               10   ;* In the following program the variable "Count" holds the octet     *
               11   ;* count from which the data byte is to be received. The valid       *
               12   ;* octet counts are: for octet 1, count = 0A2H; octet 2, count =     *
               13   ;* 0C2H; octet 3, count = 0E2H; octet 4, count = 82H. These bytes    *
               14   ;* are stored in the external data memory. The bytes are read from   *
               15   ;* the desired octet in subsequent frames until the last byte is     *
               16   ;* received. The external crystal oscillator frequency is 12.288     *
               17   ;* MHz (24 x 512 KHz).                                               *
               18   ;*********************************************************************
               19
               20
               21
00A2           22   Count    EQU     0A2H              ;Octet 1=A2,2=C2,3=E2,4=82.
               23
????           24   Cseg     at      0H
               25
0000 020100    26            LJMP    Main_Begin
               27
               28   ;*********************************************************************
               29   ;* Read_IOM_Subroutine:                                              *
               30   ;* The following subroutine happens 30 machine cycles (15 DCLs)      *
               31   ;* before the occurrence of the desired octet. The data byte is      *
               32   ;* read from port bit P3.0, 3-4 DCLs after the occurrence of the     *
               33   ;* desired octet. The data byte is stored in external memory and     *
               34   ;* the data pointer to external memory is incremented after the      *
               35   ;* byte is received over the IOM interface. The subroutine is        *
               36   ;* exited before the next compare event.                             *
               37   ;*********************************************************************
               38
               39
005B           40            Org     5BH               ;Compare 1 interrupt routine.
               41
005B           42   Write_IOM_Subroutine:              ;4 m/c for servicing the routine.
               43
005B C2BB      44            CLR     IEN1.3            ;7th m/c into the frame.
               45
```

```
005D 00      46          NOP                    ;8th m/c into the frame.
005E 00      47          NOP                    ;9th m/c into the frame.
005F 00      48          NOP                    ;10th m/c into the frame.
0060 00      49          NOP                    ;11th m/c into the frame.
0061 00      50          NOP                    ;12th m/c into the frame.
0062 00      51          NOP                    ;13th m/c into the frame.
0063 00      52          NOP                    ;14th m/c into the frame.
0064 00      53          NOP                    ;15th m/c into the frame.
0065 00      54          NOP                    ;16th m/c into the frame.
0066 00      55          NOP                    ;17th m/c into the frame.
0067 00      56          NOP                    ;18th m/c into the frame.
0068 00      57          NOP                    ;19th m/c into the frame.
0069 00      58          NOP                    ;20th m/c into the frame.
006A 00      59          NOP                    ;21st m/c into the frame.
006B 00      60          NOP                    ;22nd m/c into the frame.
006C 00      61          NOP                    ;23rd m/c into the frame.
006D 00      62          NOP                    ;24th m/c into the frame.
006E 00      63          NOP                    ;25th m/c into the frame.
006F 00      64          NOP                    ;26th m/c into the frame.
0070 00      65          NOP                    ;27th m/c into the frame.
0071 00      66          NOP                    ;28th m/c into the frame.
0072 00      67          NOP                    ;29th m/c into the frame.
0073 00      68          NOP                    ;30th m/c into the frame.
0074 00      69          NOP                    ;31st m/c into the frame.
0075 00      70          NOP                    ;32nd m/c into the frame.
             71
0076 00      72          NOP                    ;New octet.
0077 A2B0    73          MOV     C,P3.0         ;First bit read.
0079 13      74          RRC     A              ;First bit into the acc.
007A 00      75          NOP                    ;36th m/c into the frame.
             76
007B 00      77          NOP                    ;37th m/c into the frame.
007C A2B0    78          MOV     C,P3.0         ;Second bit read.
007E 13      79          RRC     A              ;Second bit into the acc.
007F 00      80          NOP                    ;40th m/c into the frame.
             81
0080 00      82          NOP                    ;41st m/c into the frame.
0081 A2B0    83          MOV     C,P3.0         ;Third bit read.
0083 13      84          RRC     A              ;Third bit into the acc.
0084 00      85          NOP                    ;44th cycle.
             86
0085 00      87          NOP                    ;45th m/c into the frame.
0086 A2B0    88          MOV     C,P3.0         ;Fourth bit read.
0088 13      89          RRC     A              ;Fourth bit into the acc.
0089 00      90          NOP                    ;48th machine cycle.
             91
008A 00      92          NOP                    ;49th m/c into the frame.
008B A2B0    93          MOV     C,P3.0         ;Fifth bit read.
???? 13      94          RRC     A              ;Fifth bit into the acc.
008E 00      95          NOP                    ;52nd cycle.
             96
```

```
008F 00        97            NOP                          ;53rd machine cycle.
0090 A2B0      98            MOV     C,P3.0               ;Sixth bit read.
0092 13        99            RRC     A                    ;Sixth bit into the acc.
0093 00       100            NOP                          ;56th machine cycle.
              101
0094 00       102            NOP                          ;57th machine cycle.
0095 A2B0     103            MOV     C,P3.0               ;Seventh bit read.
0097 13       104            RRC     A                    ;Seventh bit into the acc.
0098 00       105            NOP                          ;60th machine cycle.
              106
0099 00       107            NOP                          ;61st machine cycle.
009A A2B0     108            MOV     C,P3.0               ;Eigth bit read.
009C 13       109            RRC     A                    ;Eigth bit into the acc.
              110
009D A3       111            INC     DPTR                 ;Increment the data pointer.
009E F0       112            MOVX    @DPTR,A              ;Save the acc. at the next byte.
009F A883     113            MOV     R0,DPH               ;To compare if end of array
00A1 B8FF08   114            CJNE    R0,#0FFH,CONTI       ;Compare the high byte first.
00A4 A882     115            MOV     R0,DPL               ;Load the lower byte
                                                            for comparison.
00A6 B8FF03   116            CJNE    R0,#0FFH,CONTI       ;Compare the lower byte.
              117
00A9 900000   118            MOV     DPTR,#00H            ;Initialize the data pointer.
              119
????          120   CONTI:
00AC C2C3     121            CLR     IRCON.3
00AE D2BB     122            SETB    IEN1.3
00B0 32       123            RETI
              124
              125
              126
              127   ;*********************************************************************
              128   ;* Read_IOM_Set-up:                                                  *
              129   ;* In this program the registers are set up to allow compare to      *
              130   ;* happen at the "count" value. The PTRA unit of the SAB 80535 is    *
              131   ;* programmed in the compare mode 1. The "count" value is assigned   *
              132   ;* to the compare register 1 and the corresponding interrupt is      *
              133   ;* enabled. The Timer 2 of the PTRA unit is programmed to restart    *
              134   ;* at a value of FF80H on the arrival of the falling edge of the     *
              135   ;* FSC signal.                                                       *
              136   ;*********************************************************************
              137
              138
              139
0100          140            ORG     100H
```

```
0100          141   Main_Begin:
0100 900000   142           MOV     DPTR,#00H       ;DPTR = (start of data array).
0103 75C100   143           MOV     CCEN,#00H       ;Disable compare mode.
0106 75B0FF   144           MOV     P3,#0FFH        ;SDO, SDI lines are high.
              145
0109 75C3FF   146           MOV     CCH1,#0FFH      ;Compare register has a value
010C 75C2A2   147           MOV     CCL1,#Count     ;corresponding to the
                                                     octet desired.
010F 75CBFF   148           MOV     CRCH,#0FFH
0112 75CA80   149           MOV     CRCL,#080H      ;Reload = 0FFFFH-128 (32x4).
0115 75CDFF   150           MOV     TH2,#0FFH
0118 75CC81   151           MOV     TL2,#81H        ;To avoid compare at FF80H
0118 D2CA     152           SETB    T2CM            ;T2 in compare mode 1
011D 75C108   153           MOV     CCEN,#08H       ;Compare mode enabled
0120 D2AF     154           SETB    EAL             ;Master interrupt Bit enabled.
              155
0122 758910   156           MOV     TMOD,#10H       ;Timer1 to cause more than
0125 758DFF   157           MOV     TH1,#0FFH       ;quarter of a frame delay
0128 758BD0   158           MOV     TL1,#256-48     ;to avoid match before reload.
              159
012B          160   Start:
012B 2096FD   161           JB      P1.6,$          ;Prepare for start pulse arrival.
012E 3096FD   162           JNB     P1.6,$          ;Wait for the start pulse, 1 m/c.
0131 D28E     163           SETB    TR1             ;So far 2 m/c into the frame.
0133 308FFD   164           JNB     TF1,$           ;Wait for another 49 m/c.
              165
0138 75C81D   166           MOV     T2COM,#1DM      ;T2 auto reload from P1.5.
0139 D2B8     167           SETB    IEM1.3          ;Compare interrupt 1 enable.
              168
013B 213B     169           AJMP    $               ;Wait for a match.
              170
              171           end
ASSEMBLY COMPLETE, 0 ERRORS FOUND
```

Is it possible to dynamically change the interrupt priority in the SAB 8051 family?

Question

Background

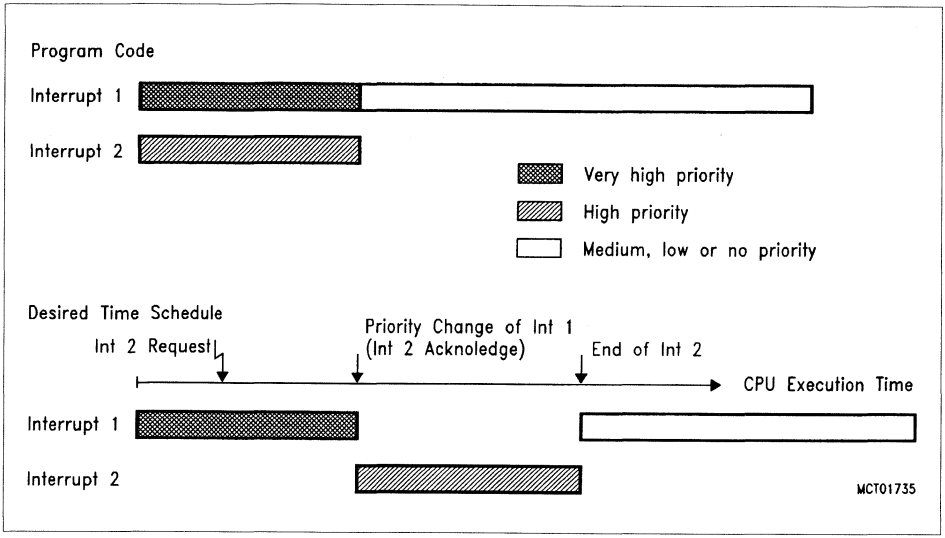
Case 1

- Several interrupts are needed
- First part of an interrupt routine needs to be of very high priority
- The rest needs only low or no priority

Case 2

- Two or three interrupts are combined to a pair / triple
- The user needs to have different priorities within this pair / triple

Situation



Desired Interrupt Handling

Reality

- The priority of an interrupt in process cannot be changed in the SAB 8051 family
- The priority of a new interrupt routine is decided at the moment of request

→ Therefore, the goal shown above cannot be reached directly!

Capabilities

Workarounds

Of course, there are other possibilities to reach the goal of dynamical change of interrupts:

1. Continuation with other priority

   The interrupt is continued with another priority
   In this case, a semaphore is necessary

2. Continuation with no priority

   The interrupt is continued as a normal subroutine

   Any enabled and requested interrupt can interrupt this "subroutine"

   This workaround can also be used for interrupts which always have the same priority (e.g. timer 0 and external interrupt 2)

Workarounds

1. Continuation with different priority

- The interrupt routine choses its new priority
- A semaphore is set in order to indicate that the interrupt is in process
- The request flag for this interrupt has to be set
- The Interrupt routine has to be left with a RETI
- After the re-entry of the interrupt depending on the semaphore the program has to branch to the next instruction after the RETI

Workaround 1

Program Example

```
Int_Entry:

        jb SEMA, GO_ON          ; if the semaphore
                                ; is set, the interrupt
                                ; routine has already
                                ; been in process

        ...                     ; part with very
        ...                     ; high priority
        ...
        mov IPx, #yy            ; change priority
        setb SEMA               ; set the semaphore
        setb IF                 ; set the request
        reti                    ; flag of this
                                ; interrupt and
                                ; return with RETI


Go_ON:                          ; re-entry address

        ...                     ; part with lower
        ...                     ; priority
        clr SEMA
        reti
```

Workaround 1 (cont'd)

2. Continuation without priority

- After the high priority part the interrupt pushes the continuation address to the stack
- Afterwards the interrupt is exited via RETI, thus releasing the current and lower priority levels
- No priority changes necessary
- The RETI instruction brings the stored target address from the stack to the program counter
- The program execution continues like a normal subroutine
- This "subroutine" has to be exited with a normal RET instruction
- This solution is also applicable for interrupt pairs, which need to be interruptable (e.g. TF0 / IEX2)

Workaround 2

Program Example

```
Int_Entry:

        ...
        ...                     ; high priority part
        ...

        push low (GO_ON)        ; store low and
        push high (GO_ON)       ; high byte in
        reti                    ; the stack
                                ; exit with a
                                ; return from
                                ; interrupt


Go_ON:                          ; re-entry address

        ...                     ; exit with a normal
        ...                     ; subroutine return
        ...
        ret
```

Workaround 2 (cont'd)

Conclusion

**With a little SW overhead
it is possible
to achieve dynamical
interrupt capabilities
for the
SAB 8051 family!**

Conclusion

Instruction Set Summary

Instruction Set Summary
8-Bit Single-Chip Microcontroller

Mnemonic		Description	Bytes	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes	Cycle
Data transfer (cont'd)				
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes	Cycle
Program and machine control (cont'd)				
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Set Summary
16-Bit Single-Chip Microcontroller

Mnemonic		Description	Bytes
Arithmetic operations			
ADD	Rw, Rw	Add direct word GPR to direct GPR	2
ADD	Rw, [Rw]	Add indirect word memory to direct GPR	2
ADD	Rw, [Rw +]	Add indirect word memory to direct GPR and post-increment source pointer by 2	2
ADD	Rw, #data3	Add immediate word data to direct GPR	2
ADD	reg, #data16	Add immediate word data to direct register	4
ADD	reg, mem	Add direct word memory to direct register	4
ADD	mem, reg	Add direct word register to direct memory	4
ADDB	Rb, Rb	Add direct byte GPR to direct GPR	2
ADDB	Rb, [Rw]	Add indirect byte memory to direct GPR	2
ADDB	Rb, [Rw +]	Add indirect byte memory to direct GPR and post-increment source pointer by 1	2
ADDB	Rb, #data3	Add immediate byte data to direct GPR	2
ADDB	reg, #data8	Add immediate byte data to direct register	4
ADDB	reg, mem	Add direct byte memory to direct register	4
ADDB	mem, reg	Add direct byte register to direct memory	4
ADDC	Rw, Rw	Add direct word GPR to direct GPR with Carry	2
ADDC	Rw, [Rw]	Add indirect word memory to direct GPR with Carry	2
ADDC	Rw, [Rw +]	Add indirect word memory to direct GPR with Carry and post-increment source pointer by 2	2
ADDC	Rw, #data3	Add immediate word data to direct GPR with Carry	2
ADDC	reg, #data16	Add immediate word data to direct register with Carry	4
ADDC	reg, mem	Add direct word memory to direct register with Carry	4
ADDC	mem, reg	Add direct word register to direct memory with Carry	4
ADDCB	Rb, Rb	Add direct byte GPR to direct GPR with Carry	2
ADDCB	Rb, [Rw]	Add indirect byte memory to direct GPR with Carry	2
ADDCB	Rb, [Rw +]	Add indirect byte memory to direct GPR with Carry and post-increment source pointer by 1	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Arithmetic operations (cont'd)			
ADDCB	Rb, #data3	Add immediate byte data to direct GPR with Carry	2
ADDCB	reg, #data8	Add immediate byte data to direct register with Carry	4
ADDCB	reg, mem	Add direct byte memory to direct register with Carry	4
ADDCB	mem, reg	Add direct byte register to direct memory with Carry	4
SUB	Rw, Rw	Subtract direct word GPR from direct GPR	2
SUB	Rw, [Rw]	Subtract indirect word memory from direct GPR	2
SUB	Rw, [Rw +]	Subtract indirect word memory from direct GPR and post-increment source pointer by 2	2
SUB	Rw, #data3	Subtract immediate word data from direct GPR	2
SUB	reg, #data16	Subtract immediate word data from direct register	4
SUB	reg, mem	Subtract direct word memory from direct register	4
SUB	mem, reg	Subtract direct word register from direct memory	4
SUBB	Rb, Rb	Subtract direct byte GPR from direct GPR	2
SUBB	Rb, [Rw]	Subtract indirect byte memory from direct GPR	2
SUBB	Rb, [Rw +]	Subtract indirect byte memory from direct GPR and post-increment source pointer by 1	2
SUBB	Rb, #data3	Subtract immediate byte data from direct GPR	2
SUBB	reg, #data8	Subtract immediate byte data from direct register	4
SUBB	reg, mem	Subtract direct byte memory from direct register	4
SUBB	mem, reg	Subtract direct byte register from direct memory	4
SUBC	Rw, Rw	Subtract direct word GPR from direct GPR with Carry	2
SUBC	Rw, [Rw]	Subtract indirect word memory from direct GPR with Carry	2
SUBC	Rw, [Rw +]	Subtract indirect word memory from direct GPR with Carry and post-increment source pointer by 2	2
SUBC	Rw, #data3	Subtract immediate word data from direct GPR with Carry	2
SUBC	reg, #data16	Subtract immediate word data from direct register with Carry	4
SUBC	reg, mem	Subtract direct word memory from direct register with Carry	4

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Arithmetic operations (cont'd)			
SUBC	mem, reg	Subract direct word register from direct memory with Carry	4
SUBCB	Rb, Rb	Subtract direct byte GPR from direct GPR with Carry	2
SUBCB	Rb, [Rw]	Subtract indirect byte memory from direct GPR with Carry	2
SUBCB	Rb, [Rw +]	Subtract indirect byte memory from direct GPR with Carry and post-increment source pointer by 1	2
SUBCB	Rb, #data3	Subtract immediate byte data from direct GPR with Carry	2
SUBCB	reg, #data8	Subtract immediate byte data from direct register with Carry	4
SUBCB	reg, mem	Subtract direct byte memory from direct register with Carry	4
SUBCB	mem, reg	Subtract direct byte register from direct memory with Carry	4
MUL	Rw, Rw	Signed multiply direct GPR by direct GPR (16-16-bit)	2
MULU	Rw, Rw	Unsigned multiply direct GPR by direct GPR (16-16-bit)	2
DIV	Rw	Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL	Rw	Signed long divide register MD by direct GPR (32-/16-bit)	2
DIVLU	Rw	Unsigned long divide register MD by direct GPR (32-/16-bit)	2
DIVU	Rw	Unsigned divide register MDL by direct GPR (16-/16-bit)	2
CPL	Rw	Complement direct word GPR	2
CPLB	Rb	Complement direct byte GPR	2
NEG	Rw	Negate direct word GPR	2
NEGB	Rb	Negate direct byte GPR	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Logical Instructions			
AND	Rw, Rw	Bitwise AND direct word GPR with direct GPR	2
AND	Rw, [Rw]	Bitwise AND indirect word memory with direct GPR	2
AND	Rw, [Rw +]	Bitwise AND indirect word memory with direct GPR and post-increment source pointer by 2	2
AND	Rw, #data3	Bitwise AND immediate word data with direct GPR	2
AND	reg, #data16	Bitwise AND immediate word data with direct register	4
AND	reg, mem	Bitwise AND direct word memory with direct register	4
AND	mem, reg	Bitwise AND direct word register with direct memory	4
ANDB	Rb, Rb	Bitwise AND direct byte GPR with direct GPR	2
ANDB	Rb, [Rw]	Bitwise AND indirect byte memory with direct GPR	2
ANDB	Rb, [Rw +]	Bitwise AND indirect byte memory with direct GPR and post-increment source pointer by 1	2
ANDB	Rb, #data3	Bitwise AND immediate byte data with direct GPR	2
ANDB	reg, #data8	Bitwise AND immediate byte data with direct register	4
ANDB	reg, mem	Bitwise AND direct byte memory with direct register	4
ANDB	mem, reg	Bitwise AND direct byte register with direct memory	4
OR	Rw, Rw	Bitwise OR direct word GPR with direct GPR	2
OR	Rw, [Rw]	Bitwise OR indirect word memory with direct GPR	2
OR	Rw, [Rw +]	Bitwise OR indirect word memory with direct GPR and post-increment source pointer by 2	2
OR	Rw, #data3	Bitwise OR immediate word data with direct GPR	2
OR	reg, #data16	Bitwise OR immediate word data with direct register	4
OR	reg, mem	Bitwise OR direct word memory with direct register	4
OR	mem, reg	Bitwise OR direct word register with direct memory	4

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Logical Instructions (cont'd)			
ORB	Rb, Rb	Bitwise OR direct byte GPR with direct GPR	2
ORB	Rb, [Rw]	Bitwise OR indirect byte memory with direct GPR	2
ORB	Rb, [Rw +]	Bitwise OR indirect byte memory with direct GPR and post-increment source pointer by 1	2
ORB	Rb, #data3	Bitwise OR immediate byte data with direct GPR	2
ORB	reg, #data8	Bitwise OR immediate byte data with direct register	4
ORB	reg, mem	Bitwise OR direct byte memory with direct register	4
ORB	mem, reg	Bitwise OR direct byte register with direct memory	4
XOR	Rw, Rw	Bitwise XOR direct word GPR with direct GPR	2
XOR	Rw, [Rw]	Bitwise XOR indirect word memory with direct GPR	2
XOR	Rw, [Rw +]	Bitwise XOR indirect word memory with direct GPR and post-increment source pointer by 2	2
XOR	Rw, #data3	Bitwise XOR immediate word data with direct GPR	2
XOR	reg, #data16	Bitwise XOR immediate word data with direct register	4
XOR	reg, mem	Bitwise XOR direct word memory with direct register	4
XOR	mem, reg	Bitwise XOR direct word register with direct memory	4
XORB	Rb, Rb	Bitwise XOR direct byte GPR with direct GPR	2
XORB	Rb, [Rw]	Bitwise XOR indirect byte memory with direct GPR	2
XORB	Rb, [Rw +]	Bitwise XOR indirect byte memory with direct GPR and post-increment source pointer by 1	2
XORB	Rb, #data3	Bitwise XOR immediate byte data with direct GPR	2
XORB	reg, #data8	Bitwise XOR immediate byte data with direct register	4
XORB	reg, mem	Bitwise XOR direct byte memory with direct register	4
XORB	mem, reg	Bitwise XOR direct byte register with direct memory	4

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Boolean bit manipulation operations			
BCLR	bitaddr	Clear direct bit	2
BSET	bitaddr	Set direct bit	2
BMOV	bitaddr, bitaddr	Move direct bit to direct bit	4
BMOVN	bitaddr, bitaddr	Move negated direct bit to direct bit	4
BAND	bitaddr, bitaddr	AND direct bit with direct bit	4
BOR	bitaddr, bitaddr	OR direct bit with direct bit	4
BXOR	bitaddr, bitaddr	XOR direct bit with direct bit	4
BCMP	bitaddr, bitaddr	Compare direct bit to direct bit	4
BFLDH	bitoff, #mask8, #data8	Bitwise modify masked high byte of bit-addressable direct word memory with immediate data	4
BFLDL	bitoff, #mask8, #data8	Bitwise modify masked low byte of bit-addressable direct word memory with immediate data	4
CMP	Rw, Rw	Compare direct word GPR to direct GPR	2
CMP	Rw, [Rw]	Compare indirect word memory to direct GPR	2
CMP	Rw, [Rw +]	Compare indirect word memory to direct GPR and post-increment source pointer by 2	2
CMP	Rw, #data3	Compare immediate word data to direct GPR	2
CMP	reg, #data16	Compare immediate word data to direct register	4
CMP	reg, mem	Compare direct word memory to direct register	4
CMPB	Rb, Rb	Compare direct byte GPR to direct GPR	2
CMPB	Rb, [Rw]	Compare indirect byte memory to direct GPR	2
CMPB	Rb, [Rw +]	Compare indirect byte memory to direct GPR and post-increment source pointer by 1	2
CMPB	Rb, #data3	Compare immediate byte data to direct GPR	2
CMPB	reg, #data8	Compare immediate byte data to direct register	4
CMPB	reg, mem	Compare direct byte memory to direct register	4

Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
Compare and Loop Control Instructions		
CMPD1 Rw, #data4	Compare immediate word data to direct GPR and decrement GPR by 1	2
CMPD1 Rw, #data16	Compare immediate word data to direct GPR and decrement GPR by 1	4
CMPD1 Rw, mem	Compare direct word memory to direct GPR and decrement GPR by 1	4
CMPD2 Rw, #data4	Compare immediate word data to direct GPR and decrement GPR by 2	2
CMPD2 Rw, #data16	Compare immediate word data to direct GPR and decrement GPR by 2	4
CMPD2 Rw, mem	Compare direct word memory to direct GPR and decrement GPR by 2	4
CMPI1 Rw, #data4	Compare immediate word data to direct GPR and increment GPR by 1	2
CMPI1 Rw, #data16	Compare immediate word data to direct GPR and increment GPR by 1	4
CMPI1 Rw. mem	Compare direct word memory to direct GPR and increment GPR by 1	4
CMPI2 Rw, #data4	Compare immediate word data to direct GPR and increment GPR by 2	2
CMPI2 Rw, #data16	Compare immediate word data to direct GPR and increment GPR by 2	4
CMPI2 Rw, mem	Compare direct word memory to direct GPR and increment GPR by 2	4
Prioritize Instruction		
PRIOR Rw, Rw	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Shift and Rotate Instructions			
SHL	Rw, Rw	Shift left direct word GPR; number of shift cycles specified by direct GPR	2
SHL	Rw, #data4	Shift left direct word GPR; number of shift cycles specified by immediate data	2
SHR	Rw, Rw	Shift right direct word GPR; number of shift cycles specified by direct GPR	2
SHR	Rw, #data4	Shift right direct word GPR; number of shift cycles specified by immediate data	2
ROL	Rw, Rw	Rotate left direct word GPR; number of shift cycles specified by direct GPR	2
ROL	Rw, #data4	Rotate left direct word GPR; number of shift cycles specified by immediate data	2
ROR	Rw, Rw	Rotate right direct word GPR; number of shift cycles specified by direct GPR	2
ROR	Rw, #data4	Rotate right direct word GPR; number of shift cycles specified by immediate data	2
ASHR	Rw, Rw	Arithmetic (sign bit) shift right direct word GPR; number of shift cycles specified by direct GPR	2
ASHR	Rw, #data4	Arithmetic (sign bit) shift right direct word GPR; number of shift cycles specified by immediate data	2
Data Movement			
MOV	Rw, Rw	Move direct word GPR to direct GPR	2
MOV	Rw, #data4	Move immediate word data to direct GPR	2
MOV	reg, #data16	Move immediate word data to direct register	2
MOV	Rw, [Rw]	Move indirect word memory to direct GPR	2
MOV	Rw, [Rw +]	Move indirect word memory to direct GPR and post-increment source pointer by 2	2
MOV	[Rw], Rw	Move direct word GPR to indirect memory	2
MOV	[-Rw], Rw	Pre-decrement destination pointer by 2 and move direct word GPR to indirect memory	2
MOV	Rw], [Rw]	Move indirect word memory to indirect memory	2
MOV	[Rw +], [Rw]	Move indirect word memory to indirect memory and post-increment destination pointer by 2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Data Movement (cont'd)			
MOV	[Rw], [Rw +]	Move indirect word memory to indirect memory and post-increment source pointer by 2	2
MOV	Rw, [Rw + #data16]	Move indirect word memory by base plus constant to direct GPR	4
MOV	[Rw + #data16], Rw	Move direct word GPR to indirect memory by base plus constant	4
MOV	[Rw], mem	Move direct word memory to indirect memory	4
MOV	mem, [Rw]	Move indirect word memory to direct memory	4
MOV	reg, mem	Move direct word memory to direct register	4
MOV	mem, reg	Move direct word register to direct memory	4
MOVB	Rb, Rb	Move direct byte GPR to direct GPR	2
MOVB	Rb, #data4	Move immediate byte data to direct GPR	2
MOVB	reg, #data16	Move immediate byte data to direct register	4
MOVB	Rb, [Rw]	Move indirect byte memory to direct GPR	2
MOVB	Rb, [Rw +]	Move indirect byte memory to direct GPR and post-increment source pointer by 1	2
MOVB	[Rw], Rb	Move direct byte GPR to indirect memory	2
MOVB	[-Rw], Rb	Pre-decrement destination pointer by 1 and move direct byte GPR to indirect memory	2
MOVB	[Rw], [Rw]	Move indirect byte memory to indirect memory	2
MOVB	[Rw +], [Rw]	Move indirect byte memory to indirect memory and post-increment destination pointer by 1	2
MOVB	[Rw], [Rw +]	Move indirect byte memory to indirect memory and post-increment source pointer by 1	2
MOVB	Rb, [Rw + #data16]	Move indirect byte memory by base plus constant to direct GPR	4
MOVB	[Rw + #data16], Rb	Move direct byte GPR to indirect memory by base plus constant	4
MOVB	[Rw], mem	Move direct byte memory to indirect memory	4
MOVB	mem, [Rw]	Move indirect byte memory to direct memory	4
MOVB	reg, mem	Move direct byte memory to direct register	4
MOVB	mem, reg	Move direct byte register to direct memory	4

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
Data Movement (cont'd)			
MOVBS	Rw, Rb	Move direct byte GPR with sign extension to direct word GPR	2
MOVBS	reg, mem	Move direct byte memory with sign extension to direct word register	4
MOVBS	mem, reg	Move direct byte register with sign extension to direct word memory	4
MOVBZ	Rw, Rb	Move direct byte GPR with zero extension to direct word GPR	2
MOVBZ	reg, mem	Move direct byte memory with zero extension to direct word register	4
MOVBZ	mem, reg	Move direct byte register with zero extension to direct word memory	4
Jump and Call operations			
JMPA	cc, caddr	Jump absolute if condition is met	4
JMPI	cc, [Rw]	Jump indirect if condition is met	2
JMPR	cc, rel	Jump relative if condition is met	2
JMPS	seg, caddr	Jump absolute to a code segment	4
JB	bitaddr, rel	Jump relative if direct bit is set	4
JBC	bitaddr, rel	Jump relative and clear bit if direct bit is set	4
JNB	bitaddr, rel	Jump relative if direct bit is not set	4
JNBS	bitaddr, rel	Jump relative and set bit if direct bit is not set	4
CALLA	cc, caddr	Call absolute subroutine if condition is met	4
CALLI	cc, [Rw]	Call indirect subroutine if condition is met	2
CALLR	rel	Call relative subroutine	2
CALLS	seg, caddr	Call absolute subroutine in any code segment	4
PCALL	reg, caddr	Push direct word register onto system stack and call absolute subroutine	4
TRAP	#trap7	Call interrupt service routine via immediate trap number	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Bytes
System Stack operations			
POP	reg	Pop direct word register from system stack	2
PUSH	reg	Push direct word register onto system stack	2
SCXT	reg, #data16	Push direct word register onto system stack und update register with immediate data	4
SCXT	reg, mem	Push direct word register onto system stack and update register with direct memory	4
Return operations			
RET		Return from intra-segment subroutine	2
RETS		Return from inter-segment subroutine	2
RETP	reg	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI		Return from interrupt service subroutine	2
System Control			
SRST		Software Reset	4
IDLE		Enter Idle Mode	4
PWRDN		Enter Power Down Mode (supposes NMI#-Pin being low)	4
SRVWDT		Service Watchdog Timer	4
DISWDT		Disable Watchdog Timer	4
EINIT		Signify End-of-Initialization on RSTOUT-pin	4
Miscellaneous			
NOP		Null operation	2

Instruction Set Summary

Notes

Data addressing modes

Rw: – Word GPR (R0, R1, . . ., R15)

Rb: – Byte GPR (RL0, RH0, . . ., RL7, RH7)

reg: – FR or GPR
(in case of a byte operation on an SFR, only the low byte can be accessed via 'reg')

reg:

mem: – Direct word or byte memory location

[. . .]: – Indirect word or byte memory location
(Any word GPR can be used as indirect address pointer, except for the arithmetic, logical and compare instructions, where only R0 to R3 are allowed)

bitaddr: – Direct bit in the bit-addressable memory area.

bitoff: – Direct word in the bit-addressable memory area.

#data: – Immediate constant
(The number of significant bits which can be specified by the user is represented by the respective index 'i')

#mask8: – Immediate 8-bit mask used for bit-field modifications.

Multiply and divide operations

The MDL and MDH registers are implicit source and/or destination operands of the multiply and divide instructions.

Branch target addressing modes

caddr: – Direct 16-bit jump target address
(Updates the Instruction Pointer)

seg: – Direct 2-bit segment address
(Updates the Code Segment Pointer)

rel: – Signed 8-bit jump target word offset address
relative to the Instruction Pointer of the following instruction

#trap7: – Immediate 7-bit trap or interrupt number.

Branch target addressing modes

cc: Symbolically specifiable condition codes

cc_UC	– Unconditional
cc_Z	– Zero
cc_NZ	– Not Zero
cc_V	– Overflow
cc_NV	– No Overflow
cc_N	– Negative
cc_NN	– Not Negative
cc_C	– Carry
cc_NC	– No Carry
cc_EQ	– Equal
cc_NE	– Not Equal
cc_ULT	– Unsigned Less Than
cc_ULE	– Unsigned Less Than or Equal
cc_UGE	– Unsigned Greater Than or Equal
cc_UGT	– Unsigned Greater Than
cc_SLE	– Signed Less Than or Equal
cc_SGE	– Signed Greater Than or Equal
cc_SGT	– Signed Greater Than
cc_NET	– Not Equal and Not End-of-Table

Hexadecimal Order

Instruction Op Codes in Hexadecimal Order, 8-Bit Single-Chip Microcontrollers

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Instruction Op Codes in Hexadecimal Order, 16-Bit Single-Chip Microcontrollers

Hex-code	Number of bytes	Mnemonic	Operands
00	2	ADD	Rw, Rw
01	2	ADDB	Rb, Rb
02	4	ADD	reg, mem
03	4	ADDB	reg, mem
04	4	ADD	mem, reg
05	4	ADDB	mem, reg
06	4	ADD	reg, #data16
07	4	ADDB	reg, #data8
08	2	ADD	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 1)
09	2	ADDB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 1)
0A	4	BFLDL	bitoff, #mask8, #data8
0B	2	MUL	Rw, Rw
0C	2	ROL	Rw, Rw
0D	2	JMPR	cc_UC, rel
0E	2	BCLR	bitoff.0
0F	2	BSET	bitoff.0
10	2	ADDC	Rw, Rw
11	2	ADDCB	Rb, Rb
12	4	ADDC	reg, mem
13	4	ADDCB	reg, mem
14	4	ADDC	mem, reg
15	4	ADDCB	mem, reg
16	4	ADDC	reg, #data16
17	4	ADDCB	reg, #data8
18	2	ADDC	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 1)
19	2	ADDCB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 1)
1A	4	BFLDH	bitoff, #mask8 #data8
1B	2	MULU	Rw, Rw
1C	2	ROL	Rw, #data4
1D	2	JMPR	cc_NET, rel
1E	2	BCLR	bitoff.1
1F	2	BSET	bitoff.1
20	2	SUB	Rw, Rw
21	2	SUBB	Rb, Rb
22	4	SUB	reg, mem
23	4	SUBB	reg, mem
24	4	SUB	mem, reg
25	4	SUBB	mem, reg
26	4	SUB	reg, #data16
27	4	SUBB	reg, #data8
28	2	SUB	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 1)
29	2	SUBB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 1)
2A	4	BCMP	bitaddr, bitaddr
2B	2	PRIOR	Rw, Rw
2C	2	ROR	Rw, Rw
2D	2	JMPR	cc_EQ, rel or cc_Z, rel
2E	2	BCLR	bitoff.2
2F	2	BSET	bitoff.2
30	2	SUBC	Rw, Rw
31	2	SUBCB	Rb, Rb
32	4	SUBC	reg, mem
33	4	SUBCB	reg, mem
34	4	SUBC	mem, reg
35	4	SUBCB	mem, reg

For notes see page ...

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
36	4	SUBC	reg, #data16
37	4	SUBCB	reg, #data8
38	2	SUBC	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
39	2	SUBCB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
3A	4	BMOVN	bitaddr, bitaddr
3B	–	-----	-----
3C	2	ROR	Rw, #data4
3D	2	JMPR	cc_NE, rel or cc_NZ, rel
3E	2	BCLR	bitoff.3
3F	2	BSET	bitoff.3
40	2	CMP	Rw, Rw
41	2	CMPB	Rb, Rb
42	4	CMP	reg, mem
43	4	CMPB	reg, mem
44	–	-----	-----
45	–	-----	-----
46	4	CMP	reg, #data16
47	4	CMPB	reg, #data8
48	2	CMP	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
49	2	CMPB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
4A	4	BMOV	bitadddr, bitaddr
4B	2	DIV	Rw
4C	2	SHL	Rw, Rw
4D	2	JMPR	cc_V, rel
4E	2	BCLR	bitoff.4
4F	2	BSET	bitoff.4

Hex-code	Number of bytes	Mnemonic	Operands
50	2	XOR	Rw, Rw
51	2	XORB	Rb, Rb
52	4	XOR	reg, mem
53	4	XORB	reg, mem
54	4	XOR	mem, reg
55	4	XORB	mem, reg
56	4	XOR	reg, #data16
57	4	XORB	reg, #data8
58	2	XOR	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
59	2	XORB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
5A	4	BOR	bitaddr, bitaddr
5B	2	DIVU	Rw
5C	2	SHL	Rw, #data4
5D	2	JMPR	cc_NV, rel
5E	2	BCLR	bitoff.5
5F	2	BSET	bitoff.5
60	2	AND	Rw, Rw
61	2	ANDB	Rb, Rb
62	4	AND	reg, mem
63	4	ANDB	reg, mem
64	4	AND	mem, reg
65	4	ANDB	mem, reg
66	4	AND	reg, #data16
67	4	ANDB	reg, #data8
68	2	AND	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
69	2	ANDB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
6A	4	BAND	bitaddr, bitaddr

For notes see page ...

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
6B	2	DIVL	Rw
6C	2	SHR	Rw, Rw
6D	2	JMPR	cc_N, rel
6E	2	BCLR	bitoff.6
6F	2	BSET	bitoff.6
70	2	OR	Rw, Rw
71	2	ORB	Rb, Rb
72	4	OR	reg, mem
73	4	ORB	reg, mem
74	4	OR	mem, reg
75	4	ORB	mem, reg
76	4	OR	reg, #data16
77	4	ORB	reg, #data8
78	2	OR	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
79	2	ORB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
7A	4	BXOR	bitaddr, bitaddr
7B	2	DIVLU	Rw
7C	2	SHR	Rw, #data4
7D	2	JMPR	cc_NN, rel
7E	2	BCLR	bitoff.7
7F	2	BSET	bitoff.7
80	2	CMPI1	Rw, #data4
81	2	NEG	Rw
82	4	CMPI1	Rw, mem
83	-	-----	-----
84	4	MOV	[Rw], mem
85	-	-----	-----
86	4	CMPI1	Rw, #data16
87	4	IDLE	
88	2	MOV	[-Rw], Rw
89	2	MOVB	[-Rw], Rb
8A	4	JB	bitaddr, rel
8B	–	-----	-----
8C	–	-----	-----
8D	2	JMPR	cc_C, rel or cc_ULT, rel
8E	2	BCLR	bitoff.8
8F	2	BSET	bitoff.8
90	2	CMPI2	Rw, #data4
91	2	CPL	Rw
92	4	CMPI2	Rw, mem
93	–	-----	-----
94	4	MOV	mem, [Rw]
95	–	-----	-----
96	4	CMPI2	Rw, #data16
97	4	PWRDN	
98	2	MOV	Rw, [Rw +]
99	2	MOVB	Rb, [Rw +]
9A	4	JNB	bitaddr, rel
9B	2	TRAP	#trap7
9C	2	JMPI	cc, [Rw]
9D	2	JMPR	cc_NC, rel or cc_UGE, rel
9E	2	BCLR	bitoff.9
9F	2	BSET	bitoff.9
A0	2	CMPD1	Rw, #data4
A1	2	NEGB	Rb
A2	4	CMPD1	Rw, mem
A3	–	-----	-----
A4	4	MOVB	[Rw], mem
A5	4	DISWDT	

For notes see page ...

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands	Hex-code	Number of bytes	Mnemonic	Operands
A6	4	CMPD1	Rw, #data16	C6	4	SCXT	reg, #data16
A7	4	SRVWDT		C7	–	-----	-----
A8	2	MOV	Rw, [Rw]	C8	2	MOV	[Rw], [Rw]
A9	2	MOVB	Rb, [Rw]	C9	2	MOVB	[Rw], [Rw]
AA	4	JBC	bitaddr, rel	CA	4	CALLA	cc, caddr
AB	2	CALLI	cc, [Rw]	CB	2	RET	
AC	2	ASHR	Rw, Rw	CC	2	NOP	
AD	2	JMPR	cc_SGT, rel	CD	2	JMPR	cc_SLT, rel
AE	2	BCLR	bitoff.10	CE	2	BCLR	bitoff.12
AF	2	BSET	bitoff.10	CF	2	BSET	bitoff.12
B0	2	CMPD2	Rw, #data4	D0	2	MOVBS	Rw, Rb
B1	2	CPLB	Rb	D1	–	-----	-----
B2	4	CMPD2	Rw, mem	D2	4	MOVBS	reg, mem
B3	–	-----	-----	D3	–	-----	-----
B4	4	MOVB	mem, [Rw]	D4	4	MOV	Rw, [Rw +#data16]
B5	4	EINIT		D5	4	MOVBS	mem, reg
B6	4	CMPD2	Rw, #data16	D6	4	SCXT	reg, mem
B7	4	SRST		D7	–	-----	-----
B8	2	MOV	[Rw], Rw	D8	2	MOV	[Rw +], [Rw]
B9	2	MOVB	[Rw], Rb	D9	2	MOVB	[Rw +], [Rw]
BA	4	JNBS	bitaddr, rel	DA	4	CALLS	seg, caddr
BB	2	CALLR	rel	DB	2	RETS	
BC	2	ASHR	Rw, #data4	DC	–	-----	-----
BD	2	JMPR	cc_SLE, rel	DD	2	JMPR	cc_SGE, rel
BE	2	BCLR	bitoff.11	DE	2	BCLR	bitoff.13
BF	2	BSET	bitoff.11	DF	2	BSET	bitoff.13
C0	2	MOVBZ	Rw, Rb	E0	2	MOV	Rw, #data4
C1	–	-----	-----	E1	2	MOVB	Rb, #data4
C2	4	MOVBZ	reg, mem	E2	4	PCALL	reg, caddr
C3	–	-----	-----	E3	–	-----	-----
C4	4	MOV	[Rw +#data16], Rw	E4	4	MOVB	[Rw +#data16], Rb
C5	4	MOVBZ	mem, reg	E5	–	-----	-----

For notes see page ...

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
E6	4	MOV	reg, #data16
E7	4	MOVB	reg, #data8
E8	2	MOV	[Rw], [Rw +]
E9	2	MOVB	[Rw], [Rw +]
EA	4	JMPA	cc, caddr
EB	2	RETP	reg
EC	2	PUSH	reg
ED	2	JMPR	cc_UGT, rel
EE	2	BCLR	bitoff.14
EF	2	BSET	bitoff.14
F0	2	MOV	Rw, Rw
F1	2	MOVB	Rb, Rb
F2	4	MOV	reg, mem
F3	4	MOVB	reg, mem
F4	4	MOVB	Rb, [Rw +#data16]
F5	–	-----	-----
F6	4	MOV	mem, reg
F7	4	MOVB	mem, reg
F8	–	-----	-----
F9	–	-----	-----
FA	4	JMPS	seg, caddr
FB	2	RETI	
FC	2	POP	reg
FD	2	JMPR	cc_ULE, rel
FE	2	BCLR	bitoff.15
FF	2	BSET	bitoff.15

Notes

1) These instructions are encoded by means of additional bits in the operand field of the instruction

x0h - x7h :	Rw, #data3	or	Rb, #data3
x8h - xBh :	Rw, [Rw]	or	Rb, [Rw]
xCH - xFh :	Rw, [Rw +]	or	Rb, [Rw +]

For these instructions, only the lowest four GPRs, R0 to R3, can be used as indirect address pointers.

Notes on the JMPR instructions

The condition code to be tested for the JMPR instructions is specified by the opcode.
Two mnemonic representation alternatives exist for some of the condition codes.

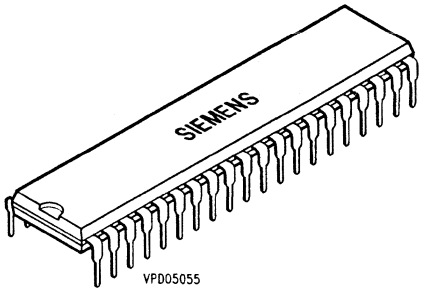
Notes on the BCLR and BSET instructions

The position of the bit to be set or to be cleared is specified by the opcode. The operand 'bitoff.n' (n = 0 to 15) refers to a particular bit within a bit-addressable word.

Notes on the undefined opcodes

A hardware trap occurs when one of the undefined opcodes signified by '-----' is decoded by the CPU.

Package Outlines

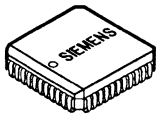


Plastic Package, P-DIP-40
(Plastic dual in-line package)
20B40 DIN 41870 T10

SMD = Surface Mounted Device

Plastic Package, P-MRFP-100
(Plastic Metric Rectangular Flat-Package – **SMD)**

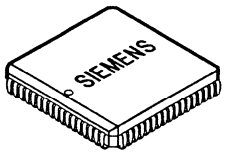
SMD = Surface Mounted Device



VPL05102

Plastic Package, P-LCC-44
(Plastic Leaded Chip Carrier) – **SMD**

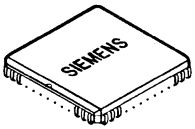
SMD = Surface Mounted Device



VPL05099

Plastic Package, P-LCC-68
(Plastic Leaded Chip Carrier) – **SMD**

SMD = Surface Mounted Device

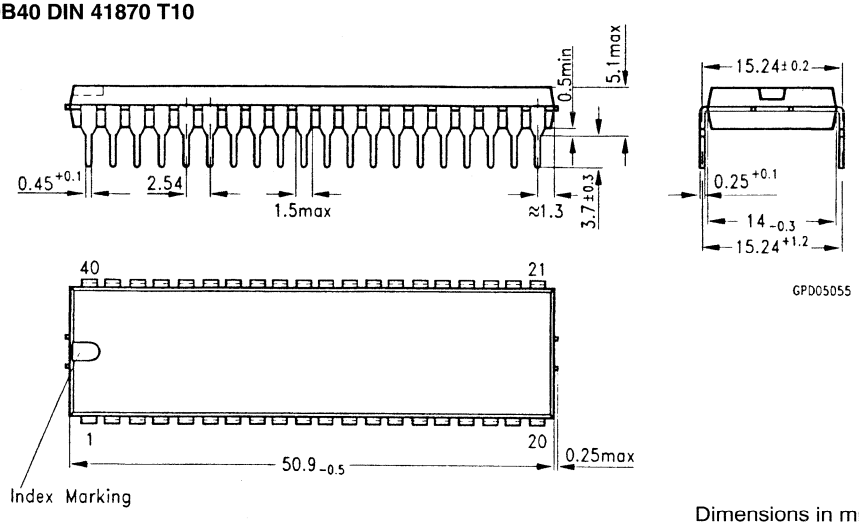


VPL05029

Plastic Package, P-LCC-84
(Plastic Leaded Chip Carrier) – **SMD**

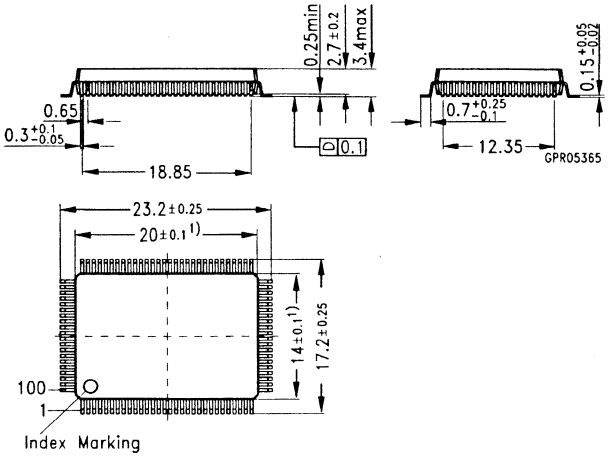
SMD = Surface Mounted Device

Plastic Package, P-DIP-40
(Plastic Dual-in-Line Pack)
20B40 DIN 41870 T10



Dimensions in mm

Plastic Package, P-MRFP-100
(Plastic Metric Rectangular Flat Package – **SMD**)

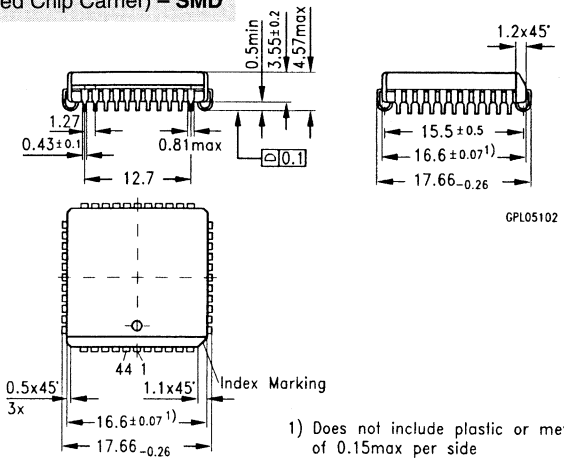


1) Does not include plastic or metal protrusions of 0.25max per side

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-44
(Plastic Leaded Chip Carrier) – **SMD**

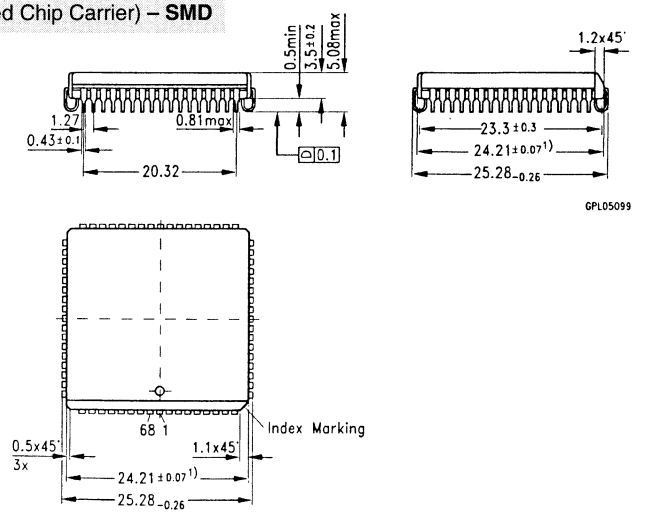


1) Does not include plastic or metal protrusions of 0.15max per side

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-68
(Plastic Leaded Chip Carrier) – **SMD**

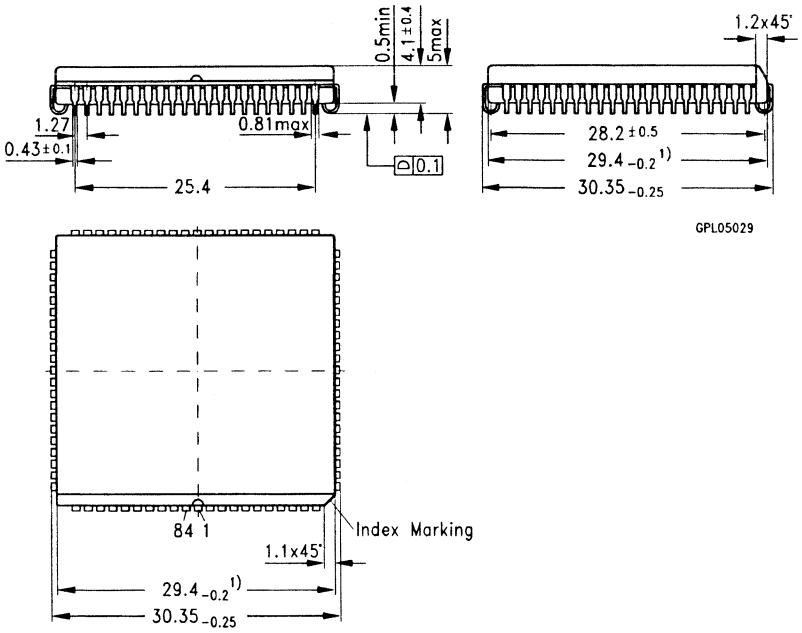


1) Does not include plastic or metal protrusions of 0.15max per side

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-84
(Plastic Leaded Chip Carrier) – **SMD**



1) Does not include plastic or metal protrusions of 0.15max per side

SMD = Surface Mounted Device

Dimensions in mm

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Information on Literature
Summary of Types in Alphanumerical Order

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Sprachenschlüssel

Englisch	-X-X-7600
Deutsch/Englisch	-X-X-7400

Inhalte der Druckschriften-Arten

Datenbuch (DB)
Sammlung der zu den Produktfamilien gehörenden Datenblätter, zusätzlich allgemeine Hinweise (Verarbeitung, Lagerung, Qualität, Anwendung).

Datenblatt (DA)
Es enthält alle für den Anwender des Halbleiters erforderlichen Angaben.

Produktschrift (PS)
Ausführliche Beschreibung zur Funktion und Anwendung der Halbleiter, z.T. mit Auszügen aus dem Datenblatt.

Themenbuch (TB)
Anwendungsorientierte Themen, z.B.
— Digitales Fernsehen
— Schaltnetzteile
— Anwendungsbeispiele
— Qualität und Zuverlässigkeit
— User's Manual.

Lieferprogramm (LM)
Überblick der lieferbaren Halbleiter. Technische Angaben beschränken sich auf das Notwendigste.

Language Code

English	-X-X-7600
German/English	-X-X-7400

Classification of Technical Publications

Data Book (DB)
Collection of Data Sheets belonging to the product families, including general notes (processing, storage, quality, application).

Data Sheet (DA)
Contains all details necessary for the user of the semiconductor.

Product Information (PS)
Detailed description of operation and application of semiconductors, sometimes with extracts from the Data Sheet.

Special Subject Book (TB)
Application-oriented subjects, e.g.
— Digital television
— Switch-mode power supplies
— Application Notes
— Quality and reliability
— User's Manual.

Short Form Catalog (LM)
Overview of semiconductors in production program. Technical details are confined to essentials.

II

Allgemeines / General

Titel Title	Bestell-Nr. Ordering Code	Art Class.	Ausgabe Edition	Seiten Pages	Preis Price
Bereich Halbleiter / Semiconductor Group					
Gehäuse- / Package Information	B192-H6636-X-X-7400	DB	05.93	400	V
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Innovation plus Excellence Semiconductor Group	B191-H6554-X-X-7600	TB	10.92	48	—
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Inhalt: Produktinformationen aus Datenbüchern, Datenblättern, Benutzer-Handbüchern, Anwendungs-Beisp., Fachaufsätzen und dem Qualitäts-Siche-rungssystem mit Tex-ten, Bildern u. Grafiken. Contents: All current product informations - text, illus-trations and graphics - from data books, data sheets, user's manuals, application notes and technical articles, plus informa-tion about the quality-assurance system.	B192-H6641-X2-X-7400	TB	10.93	—	39,-
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Summary of Types in Alphanumerical Order

Type	Ordering Code	Page
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SAB 8031A-16-P	Q 67120-C347	33
SAB 8031A-16-N	Q 67120-C349	33
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SAB 8031A-20-N	Q 67120-C467	33
SAB 8051A-P-T40/85	Q 67120-C233	33
SAB 8051A-P	Q 67120-C186	33
SAB 8051A-N	Q 67120-C224	33
SAB 8051A-16-P	Q 67120-C346	33
SAB 8051A-16-N	Q 67120-C348	33
SAB 8051A-20-P	Q 67120-C489	33
SAB 8051A-20-N	Q 67120-C490	33
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SAB 8032B-N	Q 67120-C423	53
SAB 8032B-P-T40/85	Q 67120-C427	53
SAB 8032B-16-P	Q 67120-C421	53
SAB 8032B-16-N	Q 67120-C425	53
SAB 8032B-20-P	Q 67120-C471	53
SAB 8032B-20-N	Q 67120-C472	53
SAB 8052B-P	Q 67120-C420	53
SAB 8052B-N	Q 67120-C424	53
SAB 8052B-P-T40/85	Q 67120-C428	53
SAB 8052B-16-P	Q 67120-C422	53
SAB 8052B-16-N	Q 67120-C426	53
SAB 80513-P	Q 67120-C383	53
SAB 80513-N	Q 67120-C384	53
SAB 80513-16-P	Q 67120-C441	53
SAB 80515-N	Q 67120-C211	75

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TQM

Total Quality Management

Qualität hat eine umfassende Bedeutung für uns – über das produktbezogene Verständnis hinaus. Qualität erfaßt jeden, bestimmt die Einstellung zu Kunden und Kollegen, lenkt Denken und Handeln. Unsere Mitarbeiter identifizieren sich mit diesem Qualitätsbegriff. Sie leben ihn, in der Entwicklung ebenso wie im Einkauf und in der Produktion oder den Service-Bereichen.

Wir haben unsere Auffassung von Qualität in dem Begriff Total Quality Management (TQM) zusammengefaßt. Damit sagen wir, daß Qualität erarbeitet werden muß – und daß jeder im Bereich Halbleiter dafür verantwortlich ist. TQM heißt also: Alles gleich richtig machen, dabei ständig die Leistung verbessern mit dem Ziel, „Null Fehler" zu erreichen.

In diesem Sinne ist TQM nicht nur eine Verpflichtung uns selbst gegenüber, sondern vor allem ein Versprechen an unsere Kunden: Nehmen Sie uns beim Wort, erwarten Sie mehr von uns!

Quality means many things and everything to us, far more than what is usually associated with an end-product. Nobody can get away from quality, it determines our attitude to customers and colleagues, dictates the way we think and act. Our staff identify with this kind of quality. They live it and feel it, in design and purchasing, in production and service.

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So TQM is not only an obligation that we take upon ourselves, it is also a promise to our customers. Take us up on it, expect and demand more of us.

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